Fabrication of wide-IF 200–300 GHz superconductor–insulator–superconductor mixers with suspended metal beam leads formed on silicon-on-insulator

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We report on a fabrication process that uses SOI substrates and micromachining techniques to form wide-IF SIS mixer devices that have suspended metal beam leads for rf grounding. The mixers are formed on thin 25 μm membranes of Si, and are designed to operate in the 200–300 GHz band. Potential applications are in tropospheric chemistry, where increased sensitivity detectors and wide-IF bandwidth receivers are desired. They will also be useful in astrophysics to monitor absorption lines for CO at 230 GHz to study distant, highly redshifted galaxies by reducing scan times. Aside from a description of the fabrication process, electrical measurements of these $Nb/Al–AlN_x/Nb$ trilayer devices will also be presented. Since device quality is sensitive to thermal excursions, the new beam lead process appears to be compatible with conventional SIS device fabrication technology. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1798831]

I. INTRODUCTION

Coherent detectors for millimeter and submillimeter waves are important in characterizing physical and chemical processes that occur in the earth's atmosphere and the universe. For example, molecular spectra of important species in the 63, 183, and 205 GHz bands, gathered by heterodyne mixers on NASA's Upper Atmosphere Research Satellite (UARS) Microwave Limb Sounder (MLS), has led to an understanding of ozone depletion in the earth's upper atmosphere and the global effects of pollution.[1,2] NASA's Earth Observing System (EOS) MLS, launched on the EOS Aura satellite in July 2004, improves spectral coverage to include measurements of over a dozen additional spectra in the 100 GHz to 2.5 THz range. A third generation instrument concept, the Scanning Microwave Limb Sounder (SMLS), is currently under development for a possible future satellite mission by NASA. The SMLS will have the capability to perform azimuthal scanning and with improved sensitivity, it should increase spatial coverage and extend the stratospheric measurements to the lower lying troposphere.

The UARS MLS and EOS MLS instruments use room temperature Schottky mixers. Although these mixers have been successfully applied to stratospheric chemistry, limited sensitivity and spectral bandwidth have impeded their application to tropospheric chemistry, where observational lines are pressure broadened. An infrared instrument, the Tropospheric Emissions Spectrometer, flying on EOS Aura, will provide the first substantial tropospheric chemistry observations from orbit, however infrared detection is complicated by the presence of ice clouds, dense volcanic aerosols, and smoke. An ultrasensitive microwave detector is therefore required to perform tropospheric chemistry measurements, for which superconductor–insulator–superconductor (SIS) mixers seem ideally suited. Unlike Schottky mixers whose sensitivity reaches a classical limit, the sensitivity of SIS mixers has been theoretically[3] and experimentally[4] determined to approach the quantum limit, $h\nu/k$. Besides the mixer sensitivity, a receiver with a large IF bandwidth, between 6 and 18 GHz, is required so that a larger number of atmospheric species can be monitored simultaneously in the 200–300 GHz window, which will also be conducive to the observation of weak pressure-broadened lines in the troposphere.

In the past, SIS receivers have typically been developed for astrophysics applications,[5,6] with IF bandwidths of $\sim$1–2 GHz. Increasing the IF bandwidth would also be beneficial for performing astrophysical measurements in the 200–300 GHz band. By monitoring the absorption line of CO at 230 GHz and its rotational vibrations spaced at 115 GHz, the redshift of distant galaxies can be obtained, which will be especially useful to study the 200 luminous, highly redshifted galaxies discovered recently with cameras such as SCUBA and MAMBO.[7] The wide-IF receiver would reduce scan times considerably. Since the receiver is side-band separating, it is also expected to alleviate line confusion commonly observed with double side-band mixers.

Two features in the mixer design proposed by Withington[8] and Rice[9] which promotes high IF bandwidth are the requirement for high relative permittivity (ε_r) substrates on which the mixers are fabricated, and the presence of a well-defined rf ground connection. The high ε_r helps in achieving a nearly real probe impedance that provides a good match to the waveguide without movable tuners across the entire 200–300 GHz band. Since the cut-off frequency ω_c scales as

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$$\omega_c < \frac{1}{\sqrt{\varepsilon_r}}\left[\frac{1}{a^2}+\frac{1}{b^2}\right]^{1/2},$$

where a and b are the width and thickness of a rectangular waveguide, respectively, thinner substrates are required if ε_r increases. By design, ω_c should be well above the band of interest to prevent dielectric losses through substrate modes. Silicon, with an $\varepsilon_r = 11.6$, was chosen for this work compared to the commonly used quartz substrate, which has an $\varepsilon_r = 3.8$. Besides the need for a large ε_r to maintain bandwidth, a good rf ground connection is also necessary at the perimeters of the mixer chip where it leaves its support channel and enters the waveguide. Free standing metal beams, or beam leads, are proposed as a means of achieving this well-defined rf ground. Beam leads replace wire bonding or soldering directly to the chip, reducing parasitics which become especially problematic at higher frequencies.

In this article, we present a process for fabricating these wide-IF SIS mixers with beam leads grown on thin 25 μm membranes of Si for the 200–300 GHz band. The unique features of this process are the utilization of silicon-on-insulator (SOI) substrates and micromachining techniques that are amenable to the formation of SIS mixers having suspended Au beams. By using SOI substrates, thin Si of a thickness dictated by the frequency band of operation can be obtained uniformly across a large area wafer. In the past, thin membranes of SiN_x have been used for the same purpose, but the ~ 1 μm of SiN_x was deposited using CVD.[10] Beam leads have also been employed in GaAs-based mixers and multipliers, in which case lapping was used to thin down the substrate to the desired thickness.[11,12] Silicon also has properties which are more favorable compared to quartz as the substrate thickness decreases. For example, it has a rupture modulus of 135 MPa compared to 50 MPa for quartz, and a higher thermal conductivity of 150 W/mK compared to 2 W/mK for quartz; crystalline quartz also has properties that are anisotropic. The SOI process described here replaces manual dicing of the thin mixer chips with a lithographic dicing technique. In this article, aside from a description of the fabrication process, electrical measurements of SIS devices fabricated using this process will also be presented.

II. FABRICATION PROCESS

In order to ensure optimum performance, the 3 dB roll-off frequency of the SIS mixer, $f_{3\ \mathrm{dB}} = 1/2\pi R_n C$ should be high, implying that R_nC of the junction is low; R_n and C are the normal state resistance and junction capacitance, respectively. When high current density (J_c) or thinner barrier junctions are used, the R_n decreases exponentially while C increases only linearly; high-J_c junctions thus have a net effect of decreasing R_nC. Since the mixer conversion efficiency and noise temperature are affected by the R_{sg}/R_n ratio, where R_{sg} is the subgap resistance, low leakage junctions are also desired at the same time. For this reason, AlN_x was the barrier material of choice for the wide-IF mixer work, because it is easier to form low leakage, high-J_c junctions with this material compared to AlO_x. In addition, the AlN_x barrier junctions are less sensitive to thermal excursions, which was another incentive for considering them in this fabrication process.

TABLE I. Deposition methods and layer thicknesses.

Layer	Deposition method	Thickness (nm)
SiO_2 stop layer	Wet oxidation	500
AlN_x stop layer	Reactive sputtering	10
Nb base-electrode	dc magnetron sputtering	200
Al proximity	dc magnetron sputtering	~ 6
AlN_x	rf nitridation of Al	<2
Nb counter-electrode	dc magnetron sputtering	60
SiO	Thermal evaporation	300
Wire	dc magnetron sputtering	400
Nb/Au seed	dc sputtering/thermal evaporation	7/30
Au beam lead	e-beam evaporation	1000

The fabrication process can be divided into three sections: (A) the front-side process, where the SIS devices with beam leads are formed on the SOI wafer; (B) the back-side process, where the wafer is wax-mounted onto a carrier, thinned, and the devices partitioned; and finally, (C) the release process, which encompasses the lithographic dicing technique.

A. Front-side process

The SOI wafers were obtained from BCO Technologies and had thicknesses of 25 μm for the Si device, 0.5 μm for the buried oxide (BOX) and 350 μm for the handle layers. The Nb/Al-AlN_x/Nb trilayer was deposited *in situ* in a load-locked dc magnetron sputtering system.[13] The base pressure of the system was $\sim 8\times 10^{-8}$ Pa. Prior to trilayer deposition, an etch stop layer of either thermal SiO_2 or AlN_x was deposited. The Nb base- and counter-electrodes were deposited at conditions which lead to slightly compressive film stresses, typically 300 W, and Ar pressures of 0.8 Pa. The deposition methods and thicknesses for all of the front-side process layers are summarized in Table I.

The lithography for four of the five layers in the process was conducted in a 5:1 GCA 6300 wafer stepper; the device partitioning layer was patterned using a Karl Suss MA-6 contact aligner equipped with back-side alignment, as described in Sec. II B. Test dies from a diagnostic mask set were also patterned concurrently alongside the mixer devices at certain locations on the 4 in. SOI wafer, which had single junctions ranging in size from 0.6 to 5 μm. The junction process up to wire layer (third masking layer), was performed in the standard self-aligned lift-off manner;[13] junction lithography was conducted using Shipley's 660 resist which is $\sim$400 nm in thickness.

The beam leads masking step, the fourth in the process, utilizes a bi-layer lift-off technique, which results in an easier lift-off of metal films. In this case, 950 k 5% poly(methyl methacrylate) (PMMA) was spun on the wafer and baked at 115 °C for 15 min. The beams leads lithography was done in the usual way on the stepper using Arch 620 resist and AZ 300 MIF developer. An oxygen plasma was used to remove the interfacial layer between the PMMA and the photoresist,

and the PMMA was flood exposed in deep UV radiation for 7 min. The PMMA was then developed in chlorobenzene at 30 °C for 20–30 s, and a typical undercut of ~1 μm resulted between the overlying resist. The wafer was then placed in the sputtering system and a short ion mill was performed, prior to depositing a seed layer of Nb/Au to enhance adhesion, having thicknesses as given in Table I.

After the seed layer was deposited, the Au beam leads were grown to the desired thickness in an e-beam evaporation system. A low deposition rate of ~0.5 nm/s was chosen to enhance film density. Since the base pressure was quite low $\sim 6.6\times10^{-6}$ Pa, the impurity incorporation during growth was assumed to be minimal. The Au film growth was done in two stages with a 10 min cooling step in between to minimize heating. After growth, the unwanted Au lifted-off easily in acetone at ~80 °C.

B. Back-side process

Outlined in Fig. 1 is a summary of the back-side process from the point where the SIS mixer devices with beam leads have been patterned on the front of the SOI substrates. The back-side process sequence was as follows: (1) the devices were mounted with wax onto a carrier wafer; (2) the handle was etched using deep-trench reactive ion etching (DRIE); (3) the back-side device partitioning lithography was conducted on a thin ~25 μm, wax-mounted film of Si; (4) the partitioned devices were etched using DRIE. Each of these steps is now discussed in detail.

1. Mounting

Although devices from an entire wafer could be processed for back-side patterning, initial runs used only half of the 4 in. SOI wafer, which was mounted on an optically clear carrier wafer. Sapphire was chosen over Pyrex™ due to its higher thermal conductivity, 110 W/mK compared to 0.44 W/mK, which would minimize the chance of the wax to reflow during the high-density plasma etch. Dental or sticky wax from Kerr Corporation (00625) was used for the mounting purpose, which had a flow point of ~90 °C and was soluble in toluene. First, a layer of resist (AZ 4330) was spun onto the front-side of the devices for protection. The sapphire wafer was placed on a hot plate at 115 °C and allowed to thermalize prior to applying a small quantity of dental wax in the area where the device wafer was to be mounted. The SOI wafer was then placed onto the sapphire (device-side facing down), and allowed to cool to ~50 °C as the wax hardened. Any excessive wax on the edges was then removed with toluene. The sapphire/SOI wafer assembly was then placed onto a Si-backing wafer using water soluble crystal bond wax that had a melting point of ~55 °C; the wafer was now ready for loading into the DRIE system.

2. DRIE of SOI handle

The handle of the SOI wafer was removed in a DRIE system manufactured by STS. For the handle etch, the DRIE was operated in the standard mode with SF_6 flowing at a

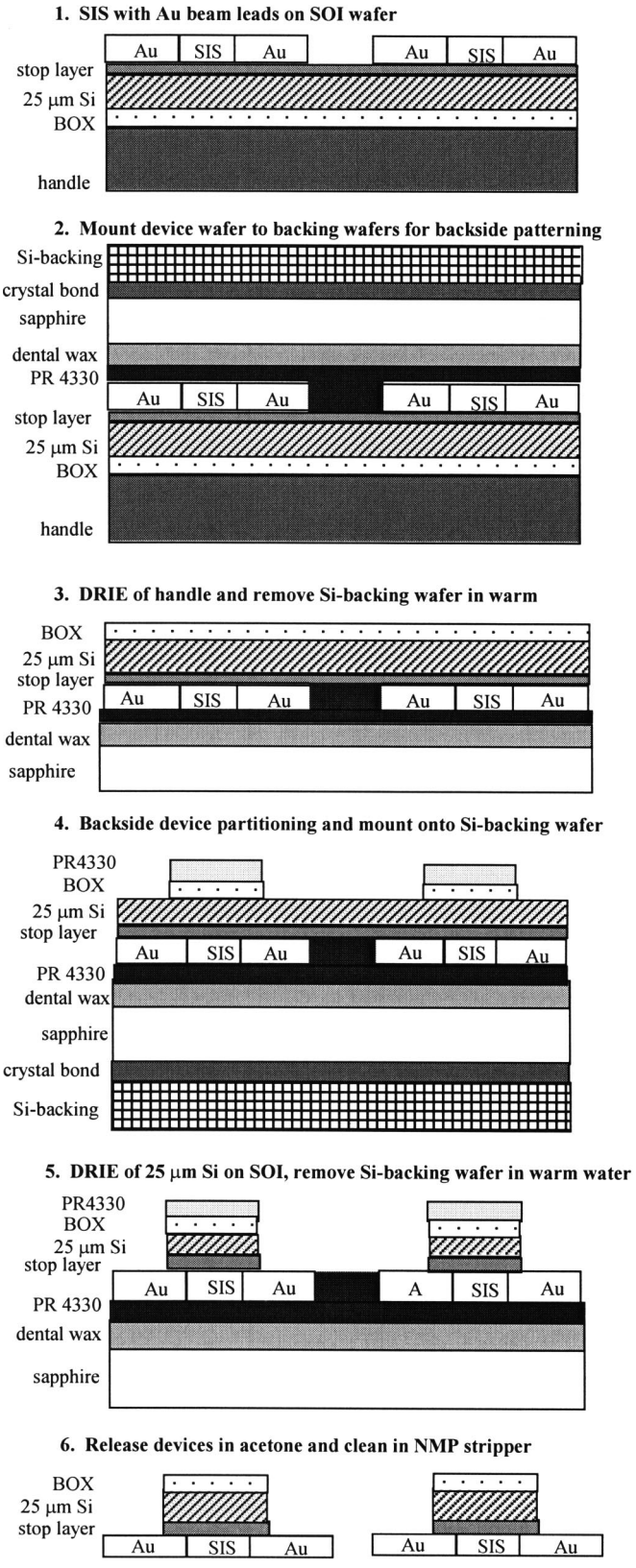

FIG. 1. Process flow depicting the back side patterning steps, after the SIS mixer devices have been fabricated on the front of the SOI wafer (not to scale).

constant rate. The fluorine-rich, high-density plasma results in a fully isotropic profile. The 350 μm of Si was etched in ~2 h 30 min and the 0.5 μm of the BOX served as an etch stop layer. The STS also has a He cooled substrate chuck, unlike conventional parallel plate etchers, which minimized substrate heating during the etch. After the handle was etched isotropically, the Si-backing wafer was removed by dissolving crystal bond in warm water.

Although DRIE was used for the isotropic etching of the handle, wet etchants could also be considered, such as tetramethyl ammonium hydroxide (TMAH) which has a higher selectivity to oxide, compared to potassium hydroxide (KOH). The main concern here is that these etchants need to be heated to ~80 °C in order to get an appreciable etch rate (~1 μm/min), which may cause the mounting wax to soften or reflow upon extended exposure to the solution. Capillary forces could also cause etchant to seep in from the edges, attacking the devices on the front-side, although mechanical fixtures are available which protect the sides of the wafer; this type of fixture however, would leave unetched Si on the perimeter of the wafer.

3. Device partitioning lithography

The BOX layer was not etched prior to performing the back-side lithography and served as a hard mask material, in addition to photoresist, when partitioning the devices; hexamethyldisilazane (HMDS) was thus used as an adhesion promoter. To prevent the wax from melting, lower temperature, longer bakes were used for soft baking the AZ 4330 resist; instead of the typical 95 °C bake for 45 s, the temperature was reduced to 50 °C and time extended to 1 h. Back-side lithography was carried out in the Karl Suss MA-6 contact aligner, which relaxes the focus tolerance requirement compared to the stepper for this wax-mounted substrate. The contact aligner was operated in the wedge correction mode where variations in the height of the wafer surface are compensated for, to some extent.

Back-side alignment was done in the standard way, where alignment marks from the mask are photographed and matched to the corresponding marks on the device-side of the wafer (hence the need for an optically clear carrier wafer). After development in AZ 300 MIF, the misalignment error was verified using an IR camera, and if the alignment was within specification, a low energy oxygen plasma clean was performed to remove any resist edge burrs that might be present after the back-side lithography process. The wafer was then mounted on the Si-backing wafer as described earlier, and was ready for the 25 μm Si etch in the STS.

4. DRIE of 25 μm *of device layer Si*

The BOX layer was etched in the STS, although buffered oxide etchant (BOE) could also be used for its removal at the expense of some undercut. To etch the ~25 μm of Si, the STS DRIE was operated in the time-multiplexed mode which results in a highly anisotropic etch profile characteristic of the Bosch process; the etching and passivating gas monomers, SF_6 and C_4F_8, respectively, are flowed independently, and the machine alternates between an etching cycle and a passivating cycle.[14] The etch step with SF_6 lasted 8 s, forming a shallow, isotropic trench in the silicon substrate. In the passivation cycle, which lasted 6 s, a protective fluorocarbon film is deposited everywhere using C_4F_8. In the subsequent etch step, ion bombardment preferentially removes the Teflon-like™ film from all horizontal surfaces, resulting in a highly anisotropic overall etch profile. The 25 μm of Si was etched in about 20–30 min. Visual end point detection was used as the pattern cleared to the Au beam leads. The stop layer, in the case of SiO_2, was removed using a CF_4/O_2 plasma etch. The Si-backing wafer was then removed by dissolving the crystal bond wax in warm water (~50 °C). Finally, an oxygen plasma was used to clean the back of the Au beam leads prior to releasing the mixer devices.

C. Device release

The sapphire wafer assembly was placed in acetone at 50 °C for about 2 h, which slowly removed the front-side protection resist and released the devices; the released devices were then placed in the more aggressive *N*-methyl-pyrrolidone (NMP) based stripper at 80 °C which removed any residual resist after the DRIE device-partitioning etch. Although dental wax could be dissolved directly in warm toluene to release the devices, the acetone release approach was found to leave less residue on the chips. The released devices were then soaked in IPA. Since the devices separate into individual mixer chips, the device partitioning lithography and release step comprise the lithographic dicing technique characteristic of this process, which replaces manual dicing usually necessary for thin quartz devices.

III. RESULTS AND DISCUSSION

A SEM image of a released Nb/Al-AlN_x/Nb mixer device is shown in Fig. 2, exhibiting the probe area and a side view of the beam leads. The Au beams appear straight and show no signs of stress release, which is also evident from the close-up image in Fig. 2(b). Beams thicker than ~1 μm could be grown using e-beam evaporation, but for significantly thicker leads, plating might be considered as an alternative growth technique due to its inherently higher deposition rate. The higher deposition rate implies the growth is occurring further from equilibrium, which may compromise film density, although it is not clear if this would influence rf performance to a noticeable degree. Plating has been explored extensively by Bass *et al.* for beam lead growth that resulted in thicknesses up to 10 μm.[15]

Since two types of etch-stop layers were considered, thermal SiO_2 and sputtered AlN_x, the surface quality on the back of the Au leads was distinctly different in the two cases. A "grassy" or "nano-pillar" type structure was observed on the back of the beam leads that were fabricated on SOI wafers having the SiO_2 stop layer, as shown in Fig. 3(a). The main purpose of the SiO_2 was to serve as an etch stop layer during DRIE of the device partitioning step, and when it was dry etched in a conventional RIE system using CF_4/O_2, the sur-

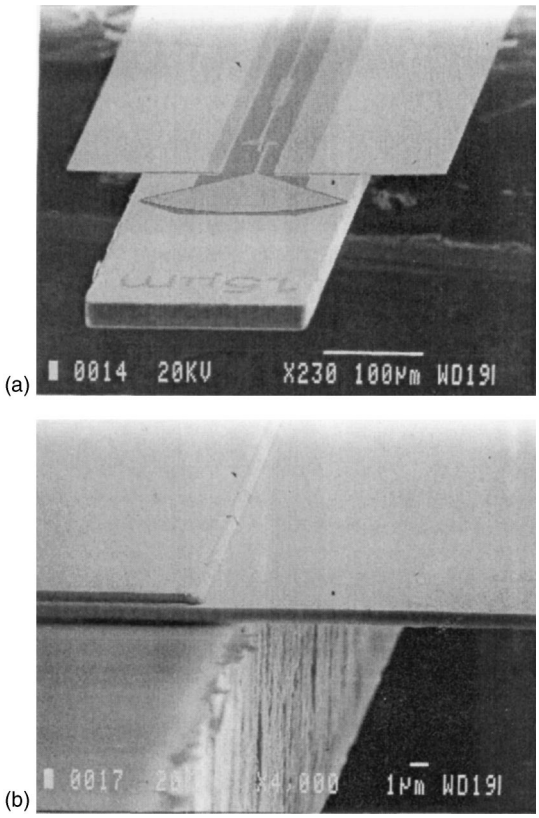

FIG. 2. (a) Front view of wide-IF SIS mixer with beam leads; (b) close-up image of beam lead area.

face was decorated with nano-pillars having widths of less than a few hundred nanometers. This surface morphology is nonideal for device applications since it would affect the electrical contact and thus rf performance. On the other hand,

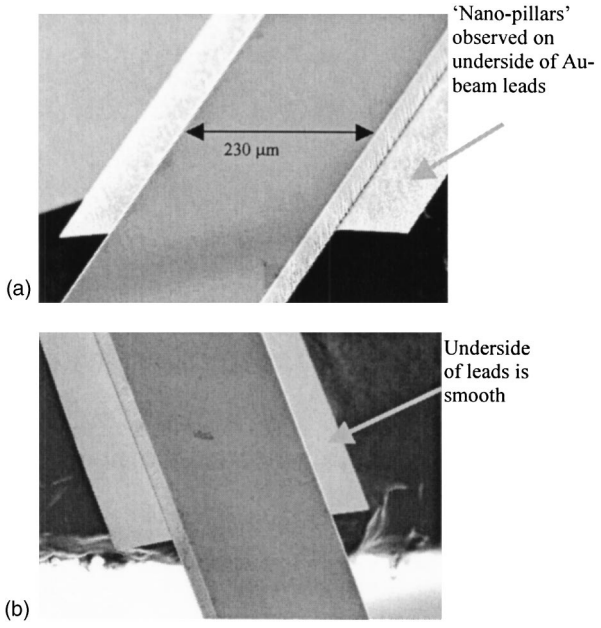

FIG. 3. Back of beam leads for mixers grown on SOI wafers with an (a) SiO_2 stop layer, and (b) AlN_x stop layer.

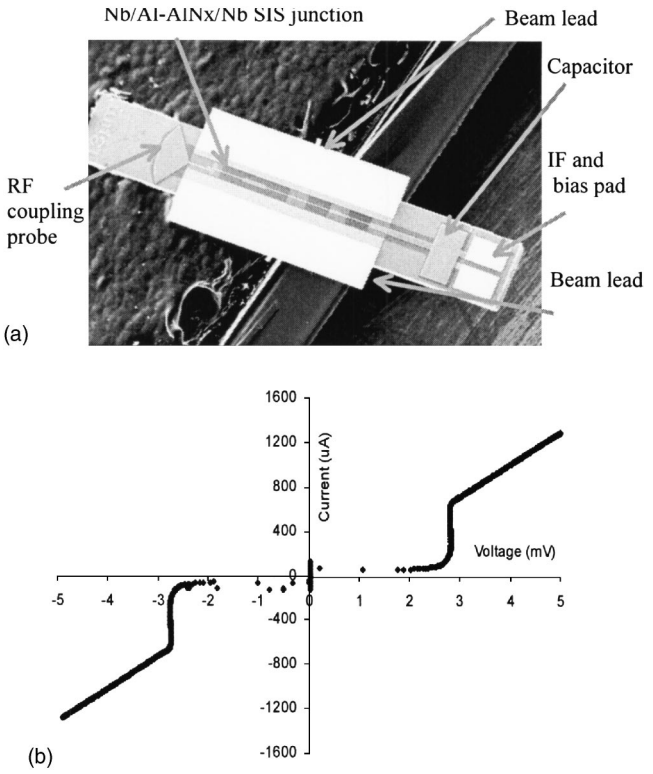

FIG. 4. (a) Micrograph of entire mixer chip; (b) $I-V$ characteristic of a junction measured from the mixer chip; junction area is 1.3 μm.

when SOI wafers with a AlN_x stop layer were used, the oxide etch was eliminated and the back of the leads was smooth, as shown in Fig. 3(b).

Test junctions were measured from a diagnostic chip that was also released in the same fashion as the mixer devices. The R_nA of these devices was determined to be $\sim$4.3 ($J_c \sim 44$ kA/cm^2) with a maximum R_{sg}/R_n ratio $\sim$10. The gap voltage, V_g, was $\sim$2.76 mV, and the junctions exhibited some heating at the voltage step due to the low-R_nA. The R_nA was calculated from the slope of the junction linear dimension d vs $1/\sqrt{R_n}$ plot, which is a fit to the Ambegaokar–Baratoff result. This approach for determining R_nA encompasses the statistical variation from junction-to-junction and is an accurate measure of R_nA. The R_nA on a diagnostic chip was measured prior to back-side thinning and compared to another test chip on the same wafer that had undergone back-side etching. No significant change in quality or R_nA was observed as a result of the back-side thinning process. This indicates the temperature rise in the DRIE plasma process is well below 200 °C, beyond which degradation in device quality of these AlN_x barrier junctions would be apparent.

A micrograph of an entire mixer chip is shown in Fig. 4(a), which depicts the rf coupling probe, capacitor, and IF and bias pads. For the present design, an alignment tolerance of 9 μm is necessary at the two edges of the 36 Ω probe area. With this wax-mounted back-side lithography technique, alignment to within a few microns was easily attainable. Shown in Fig. 4(b) is an $I-V$ characteristic of an un-

pumped junction measured from an actual mixer device with a 1.3 μm junction, having an $R_n \sim 3.8\ \Omega$. Preliminary rf measurements on other devices have resulted in double sideband mixer noise temperatures of ~ 70 K, and these results will be reported in detail elsewhere.[16]

This wax-mounted back-side lithography technique for forming beam leaded SIS mixer devices should be scalable to higher frequencies which is necessary, for example, in the SMLS to operate in the 600 GHz band. For this to occur, the thickness of the device Si must be reduced from 25 to ~ 8 μm, since $f_{3\ \mathrm{dB}} < 1/t$, where t is the thickness of the substrate; SOI wafers with this device layer thickness are easily obtainable.

In addition to wax-mounting techniques for forming the beam leads, other approaches can also be considered such as a completely front-side process. This has been explored by Bass *et al.*[15] for quartz substrates. The all-front-side process consists of fewer fabrication steps but the challenge lies in finding suitable planarizing layers after the devices have been partitioned at the outset.

Although in the present design beam leads were only chosen for rf grounding, wire bonding is still necessary to contact the IF and bias pads; beam leads could also be used for these pads, further reducing parasitics, as well as assembly time. When many mixer devices are to be assembled and mounted into waveguides as in large array telescopes like ALMA[17] which requires 64 receivers at several channels, it is conceivable that the waveguides themselves, along with the mixers, are micromachined and batch fabricated using a hybrid of the SOI process. This would reduce assembly time considerably, increasing throughput and could be a consideration for future work.

IV. CONCLUSION

A fabrication process was described that employed SOI substrates and micromachining techniques for the realization of wide-IF SIS mixer devices having suspended metal beam leads for rf grounding. Measurements of devices from diagnostic chips as well as receiver devices yielded electrical functional devices, indicating the beam lead process is compatible with conventional SIS device processing.

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