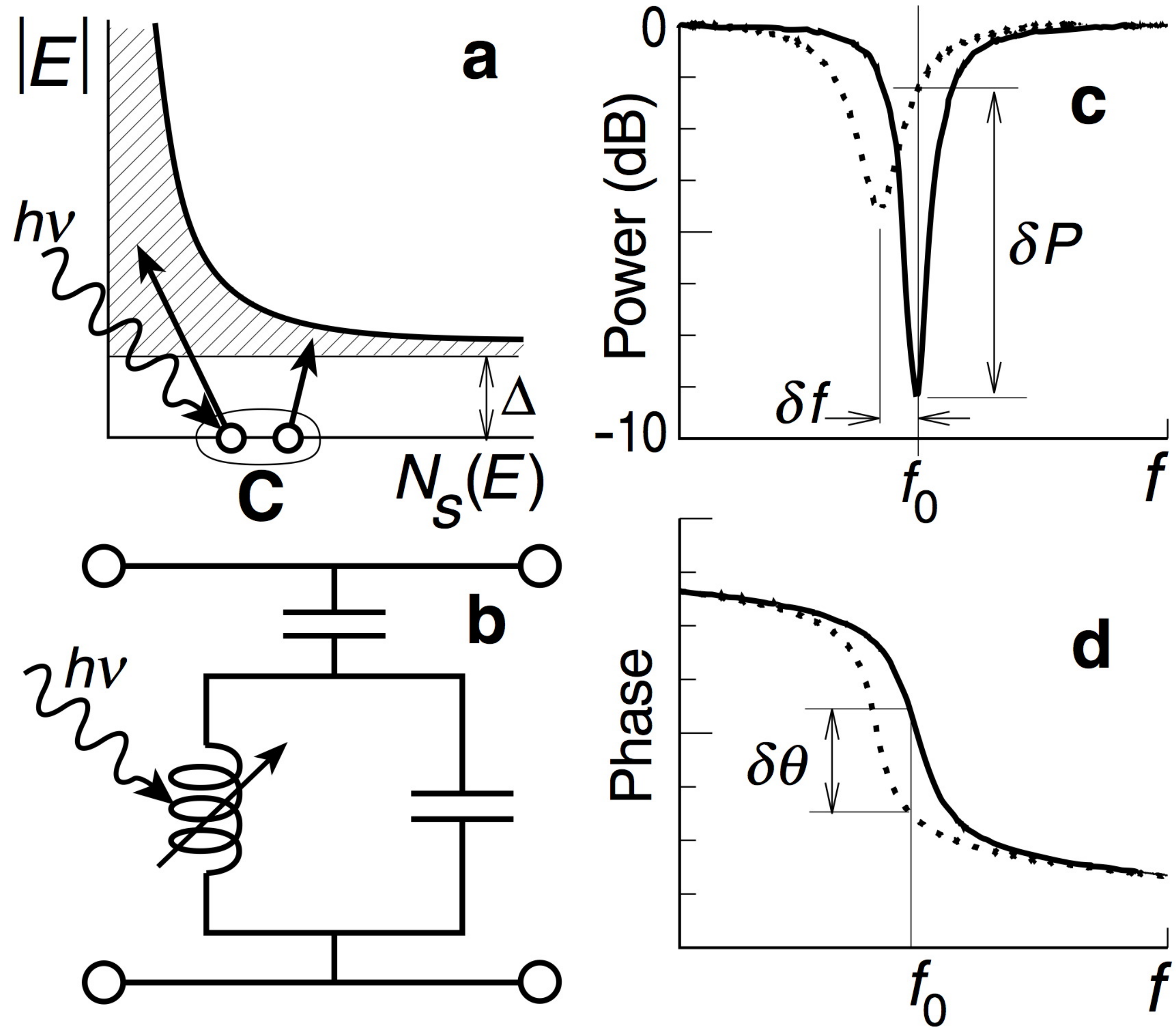
Considerations for digital readouts for a submillimeter MKID array camera

Jonas Zmuidzinas

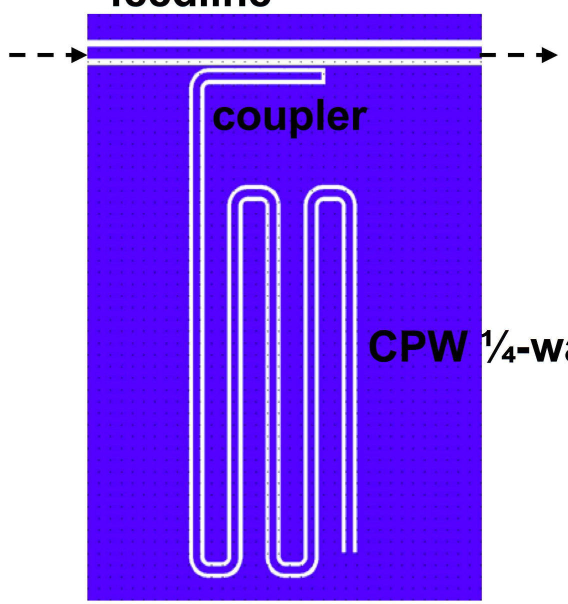
Division of Physics, Mathematics, and Astronomy

Caltech

MKID: basic principle

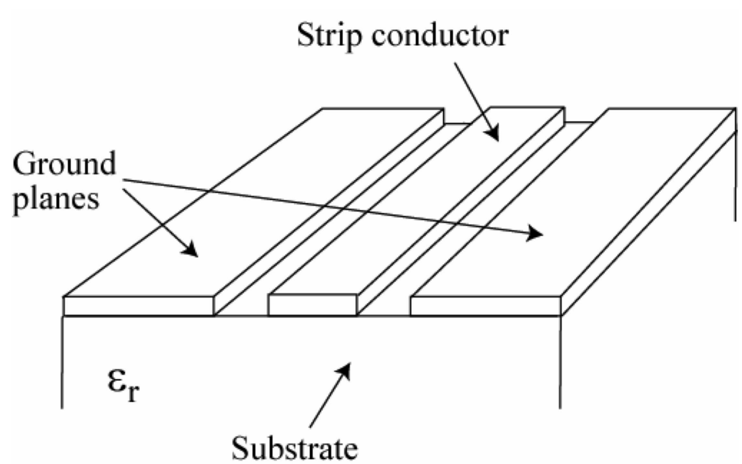


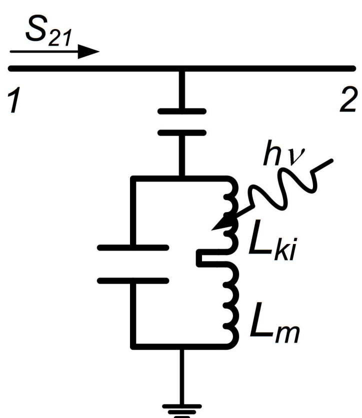
Coplanar waveguide (CPW) resonators

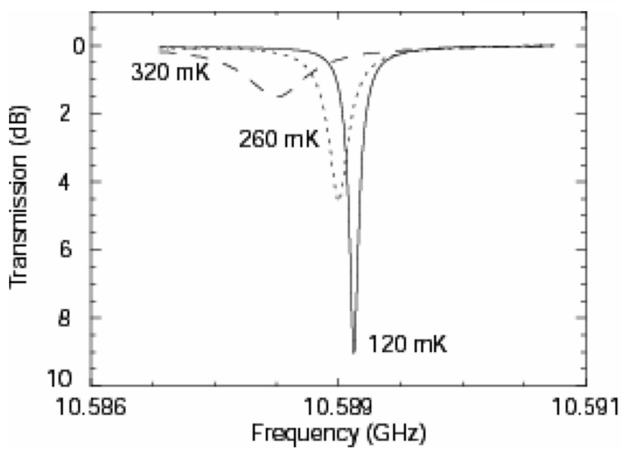


CPW resonators:

- simple one layer construction
- lack of thin-film dielectrics



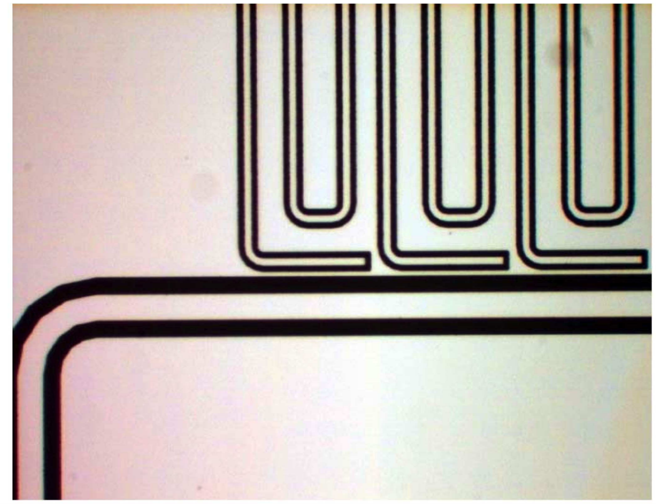


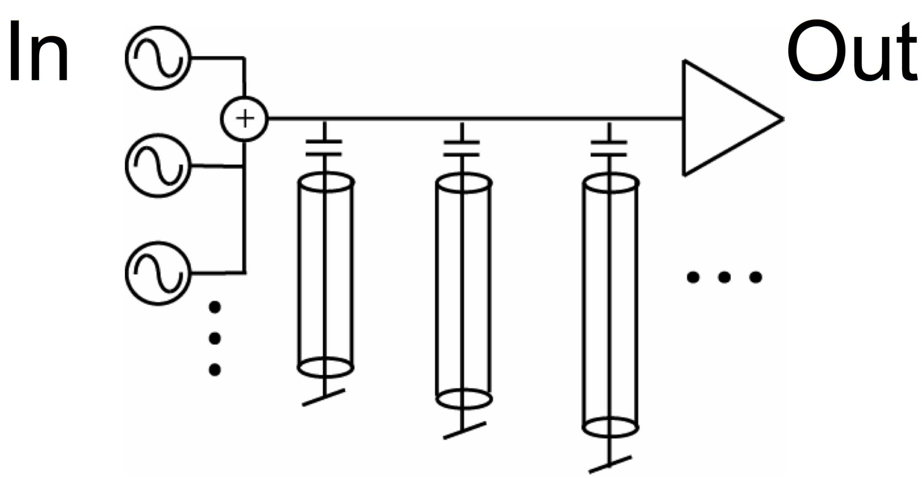


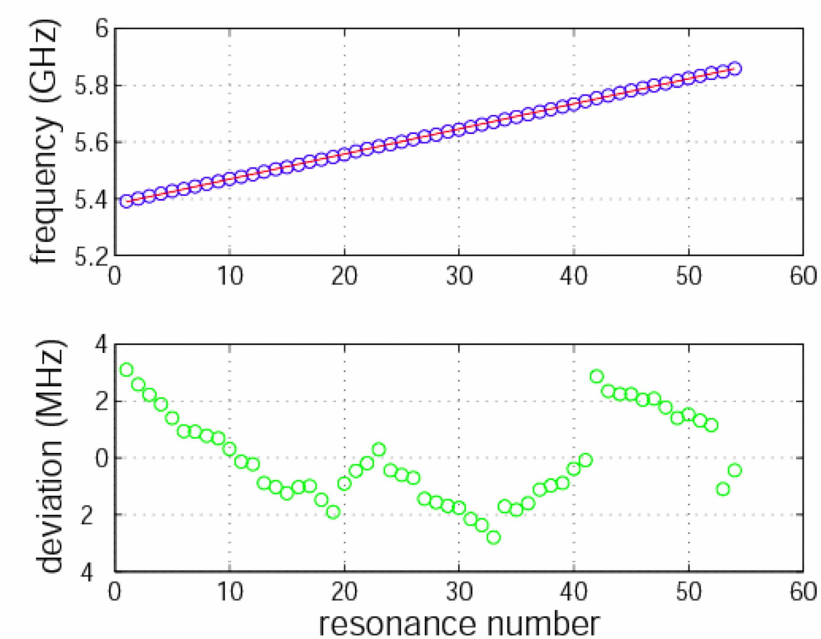
CPW Al on Sapphire
200nm thick, V = 2000μm^3,
L = 3mm, f_{res} = 10 GHz,
Q = 55,000

Frequency multiplexing

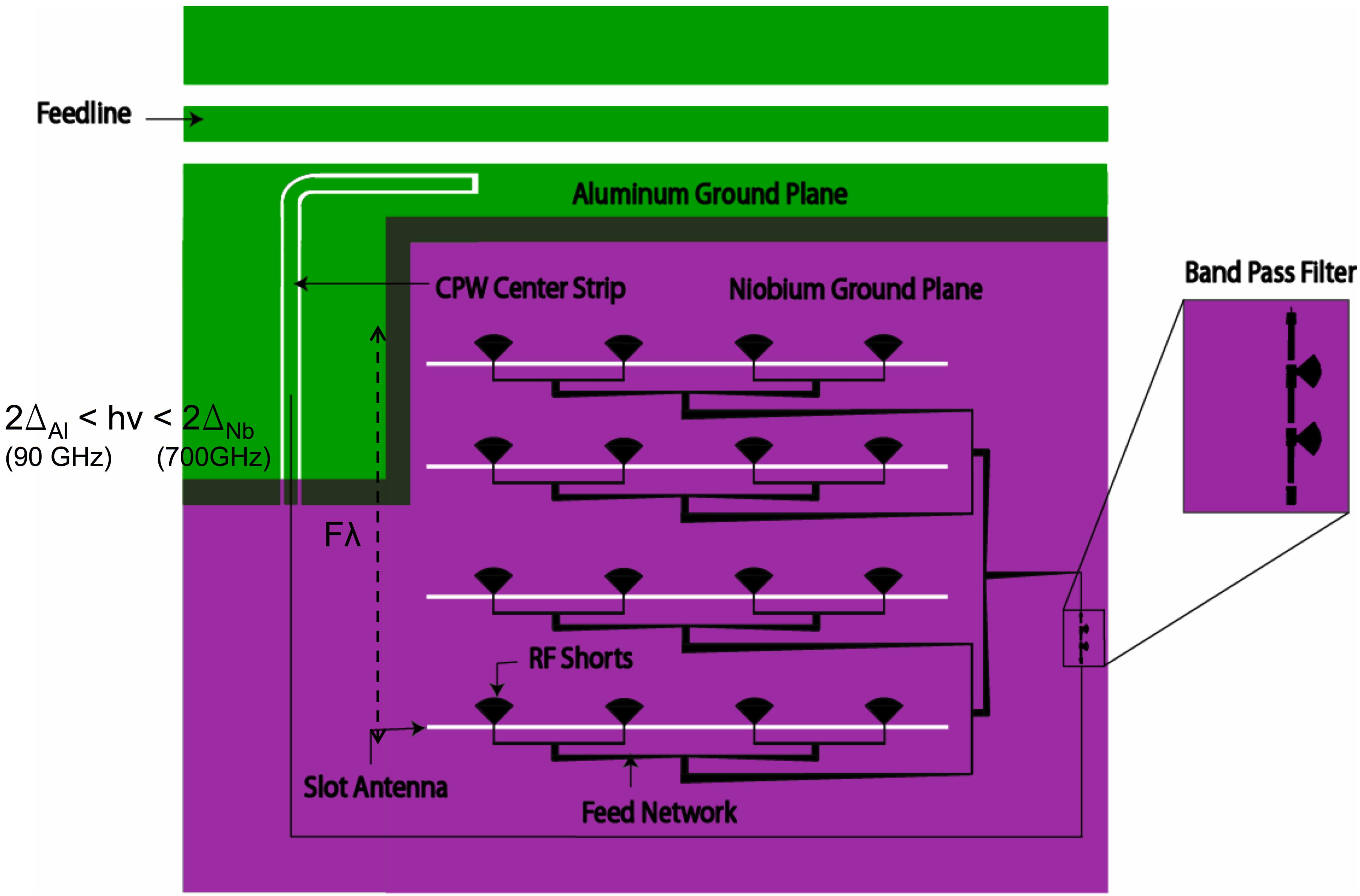
- Powerful multiplexing strategy
  - *Many detectors are coupled to a single feedline*
- Many channels per microwave amplifier
- Only cryogenic hardware: a pair of coaxes, and a wide-band LNA amplifier.



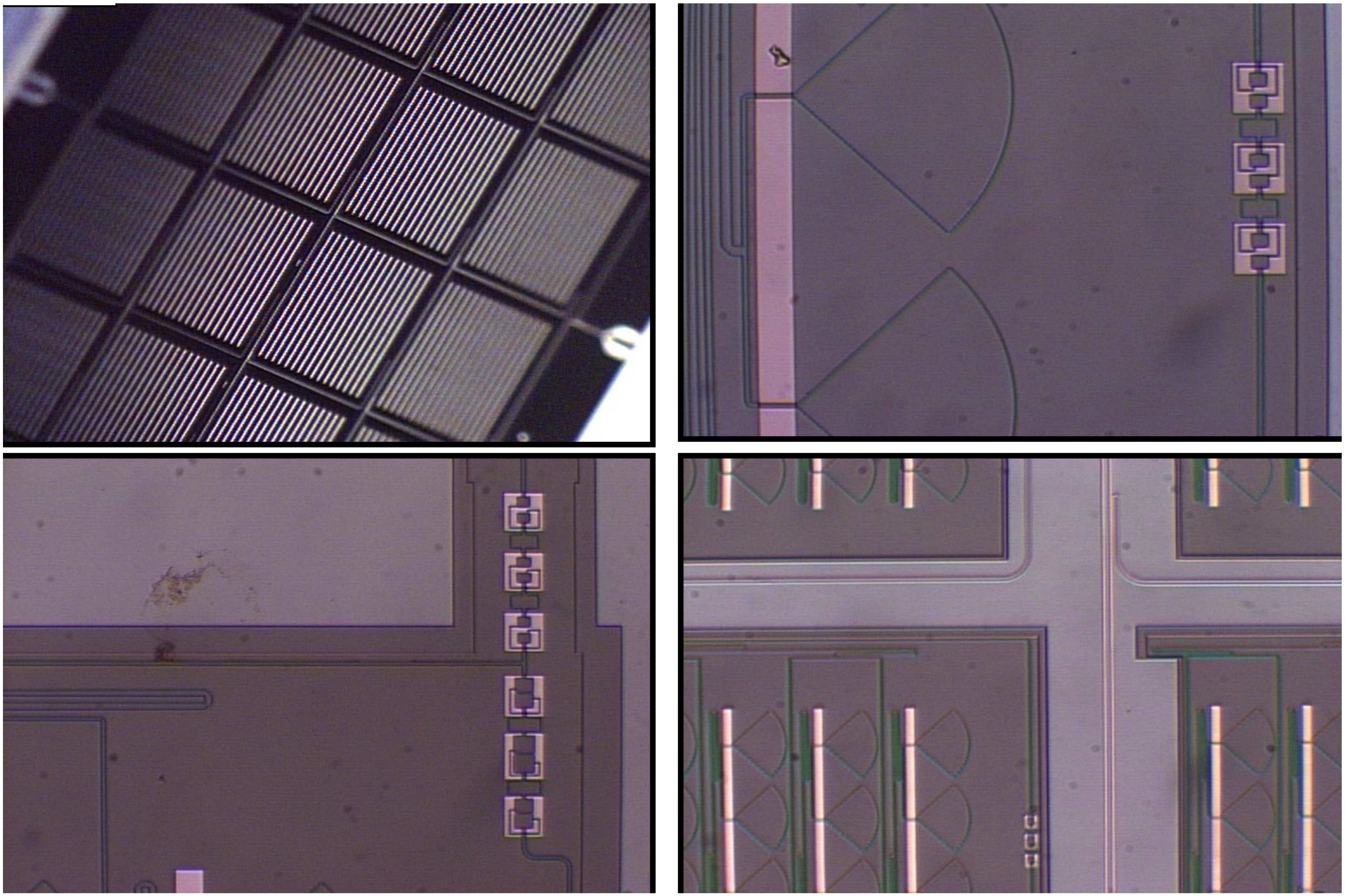




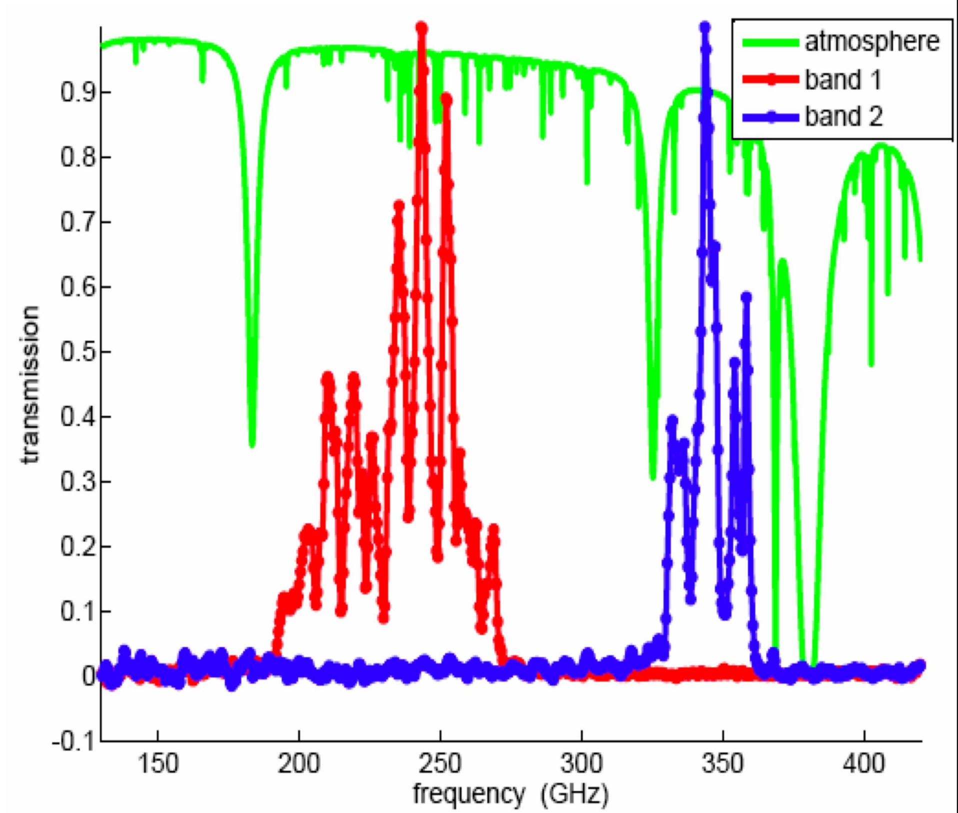
Antenna-coupled submillimeter-wave MKID



4×4 dual-color submm MKID array

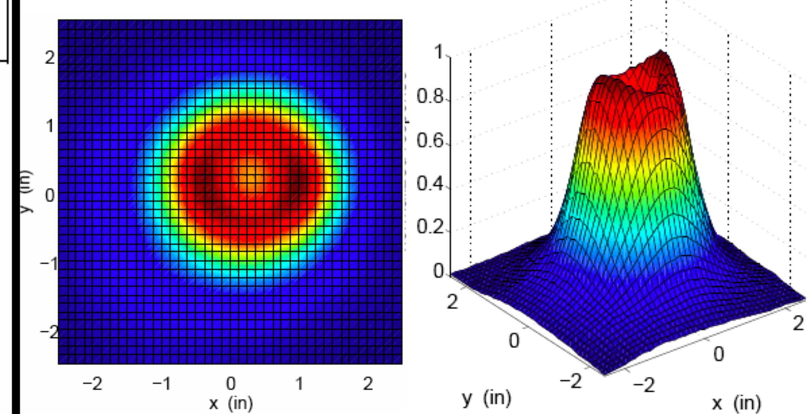


Frequency response and antenna patterns

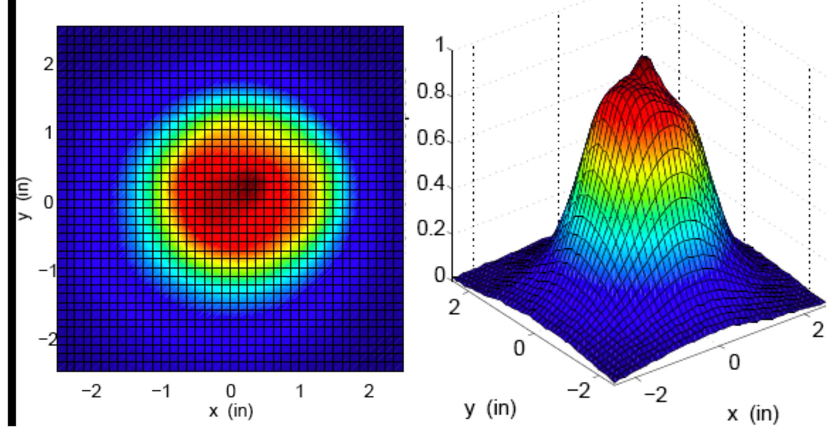


(Taken *before* Zitex AR coating applied on PTFE filters/lens)

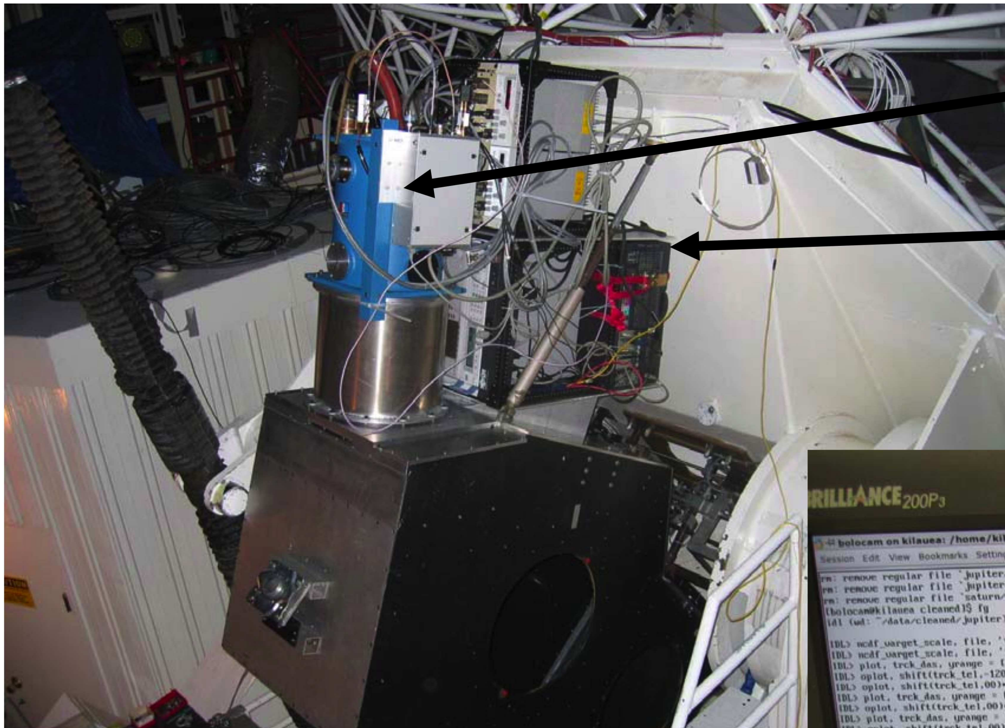
Band1



Band2



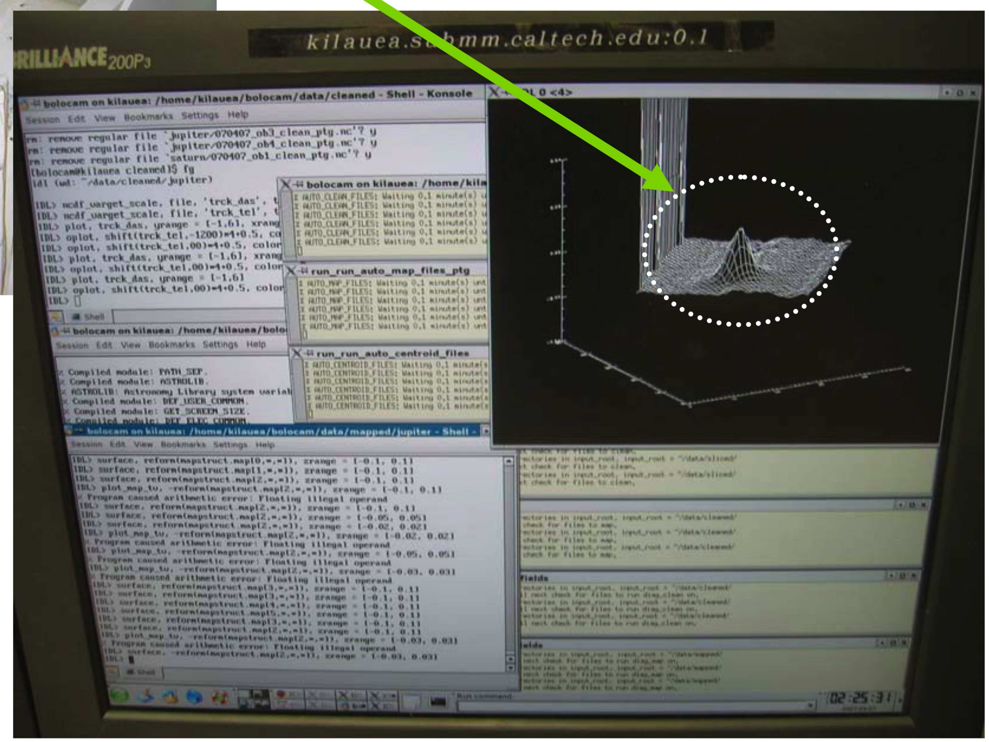
Demo at the Caltech Submillimeter Observatory (CSO)



DemoCam dewar mounted on optics box

Instrument racks

First light: detection of Jupiter with MKIDs!

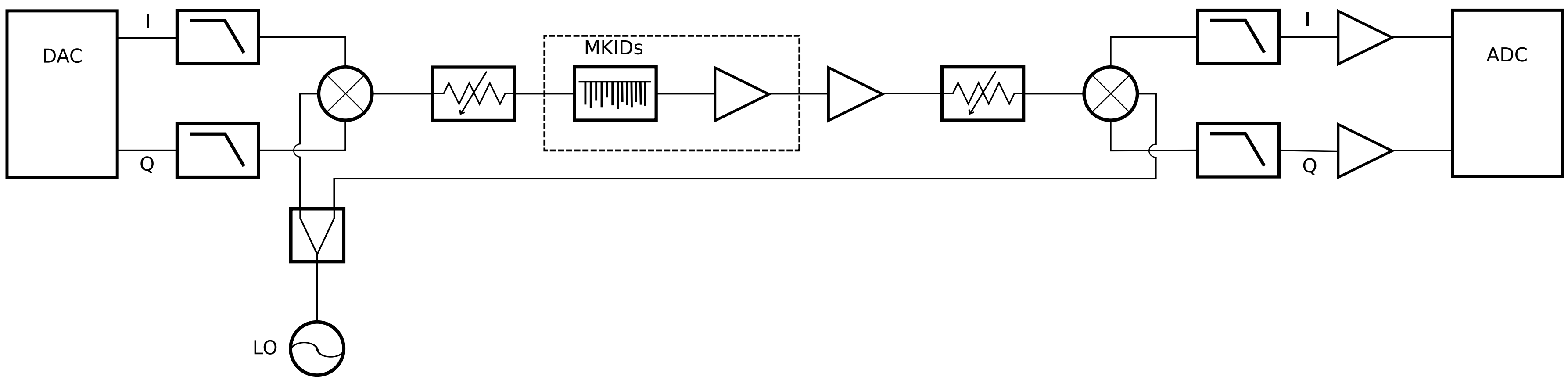


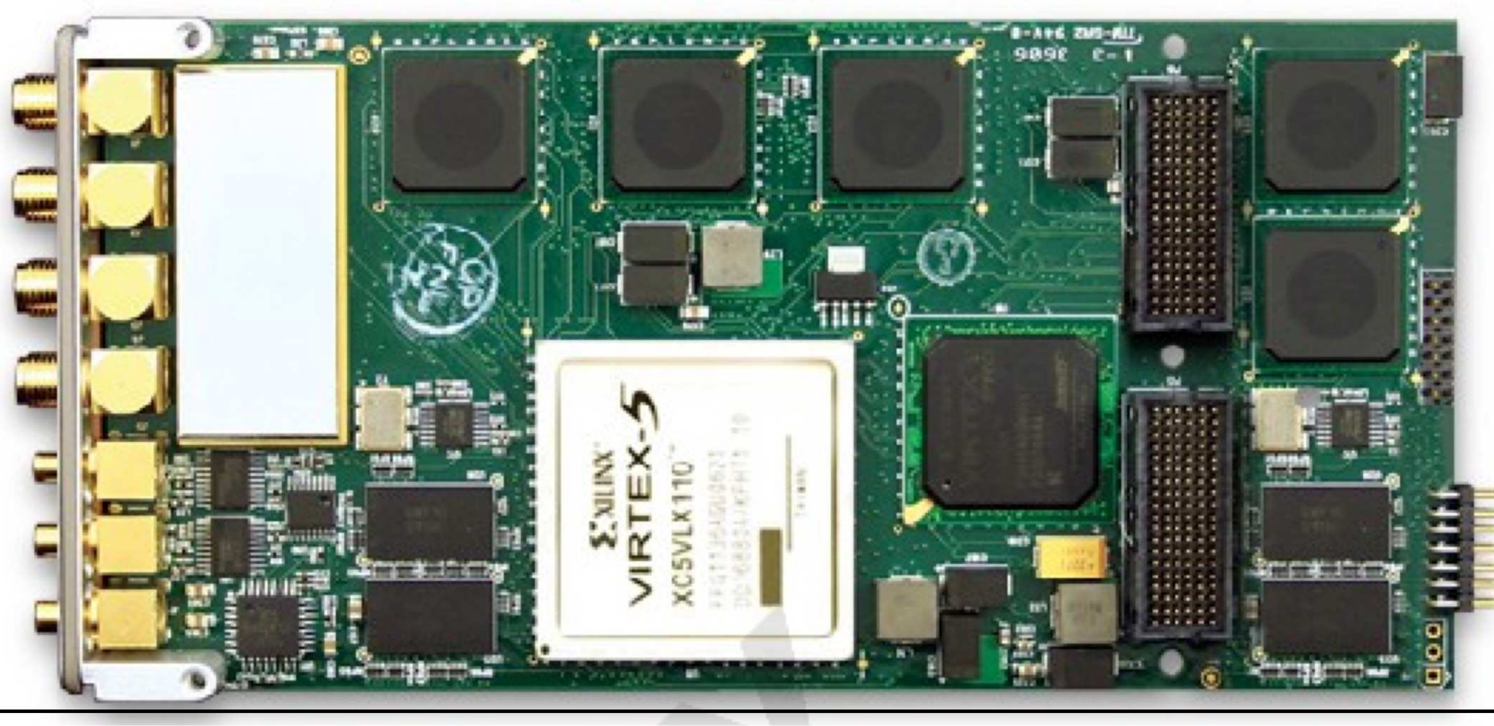
Future plans: build a 600 pixel, multi-color camera.

The MKID camera for the CSO (NSF ATI + Moore)

- Jason Glenn, PI; Sunil Golwala, co-PI
- 24×24 array $=$ 576 spatial pixels
- Four colors/bands: $\lambda =$1.3, 1.1, 0.85, and 0.75 mm
- $576 \times 4 = 2304$ MKID resonators
- Focal plane: 4×4 mosaic of 6×6 ($\times 4$) tiles
- Each $6 \times 6 \times 4$ tile has 144 MKIDs total
- 2.8 MHz per MKID $\rightarrow$ 400 MHz bandwidth per tile

Proposed 400 MHz bandwidth digital readout scheme





Issues to consider

- Digital signal processing algorithm in FPGA
- Frequency selection, output data rate
- Noise
- Dynamic range
- Spurious frequencies, intermodulation products, etc.
- Implementation details: location, packaging, power source, communication, computer interface, etc.

Digital downconverter (DDC)

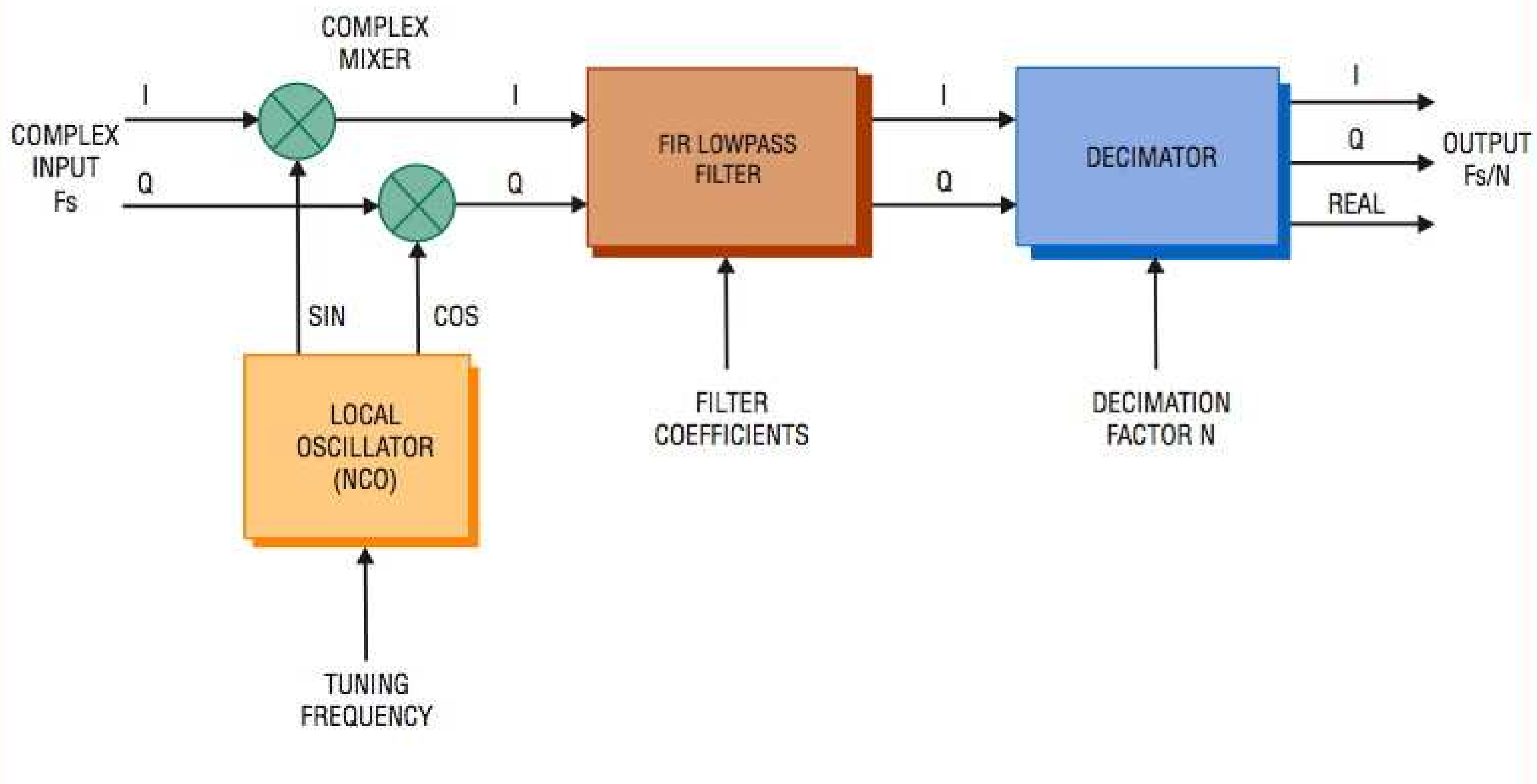


Figure 1. Digital Downconverter Block Diagram

Disadvantage: DDCs are "silicon intensive", difficult to pack lots of channels onto FPGA.

FFT Channelizer

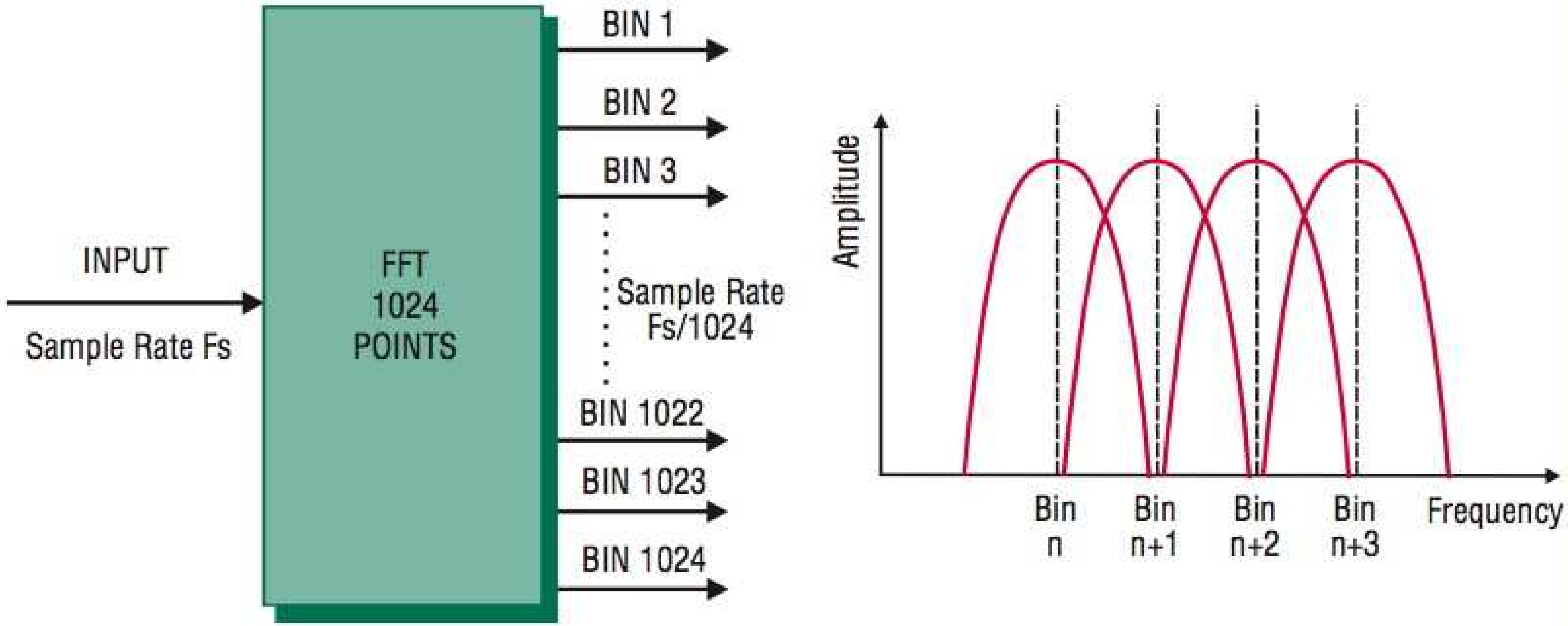


Figure 2. FFT Implementation of Channelizer

Advantage: FFT computation scales $N \log(N)$. FPGAs are capable of real-time 32k point FFTs at input data rates 2 GSamples/sec.

Disadvantage: sinc(x) sidelobes, wide output bandwidth.

A better channelizer (Pentek)

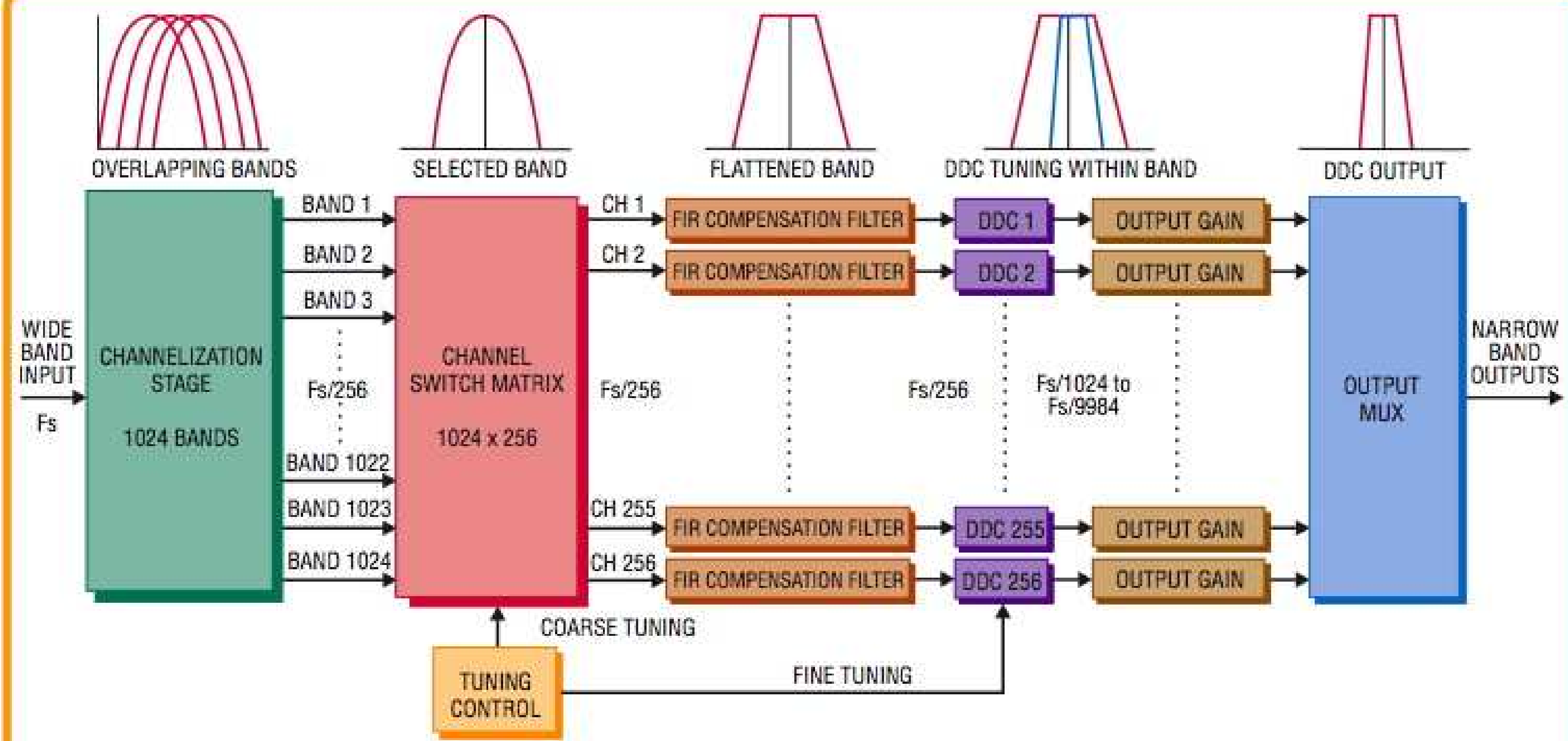
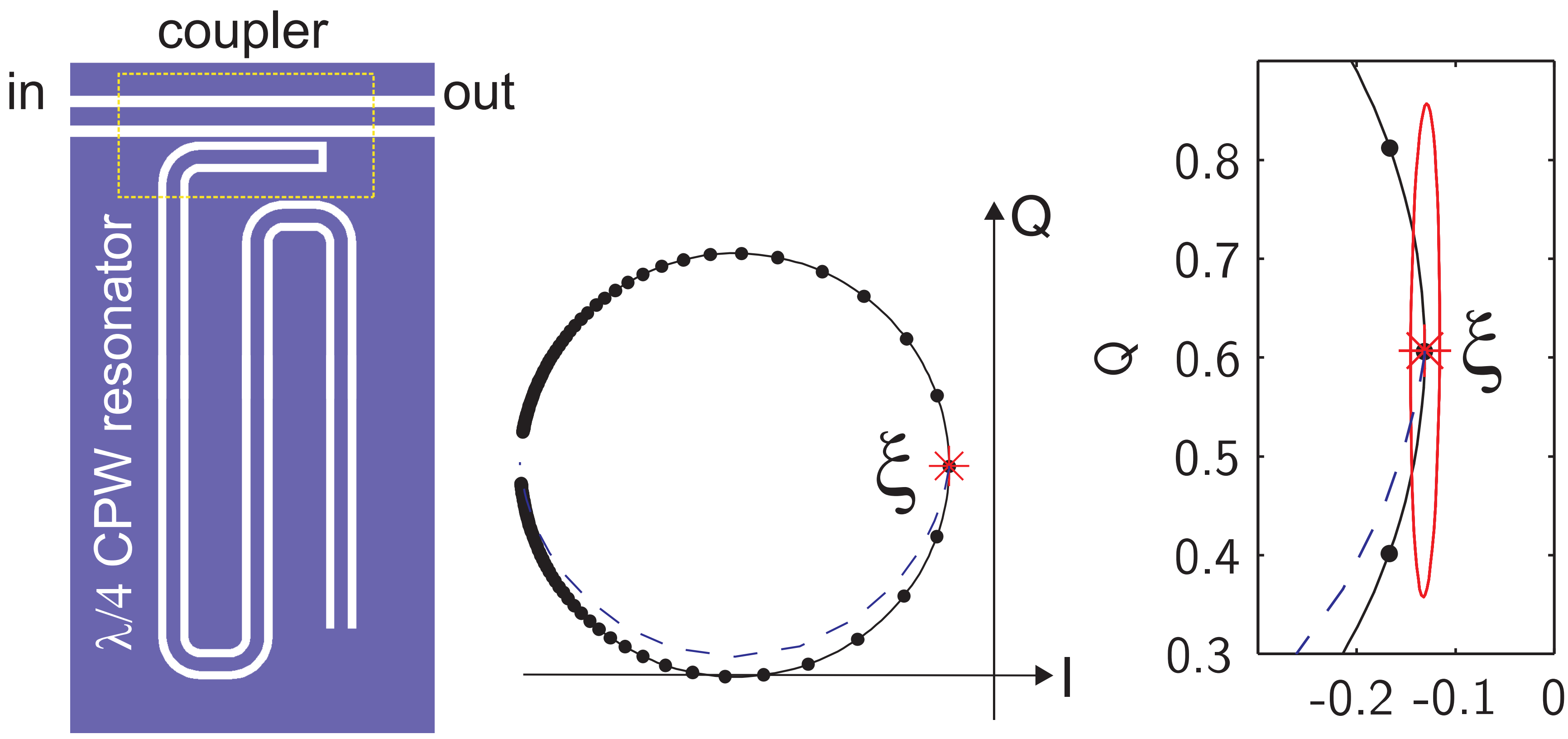


Figure 3. FPGA-based 256-Channel DDC IP Core

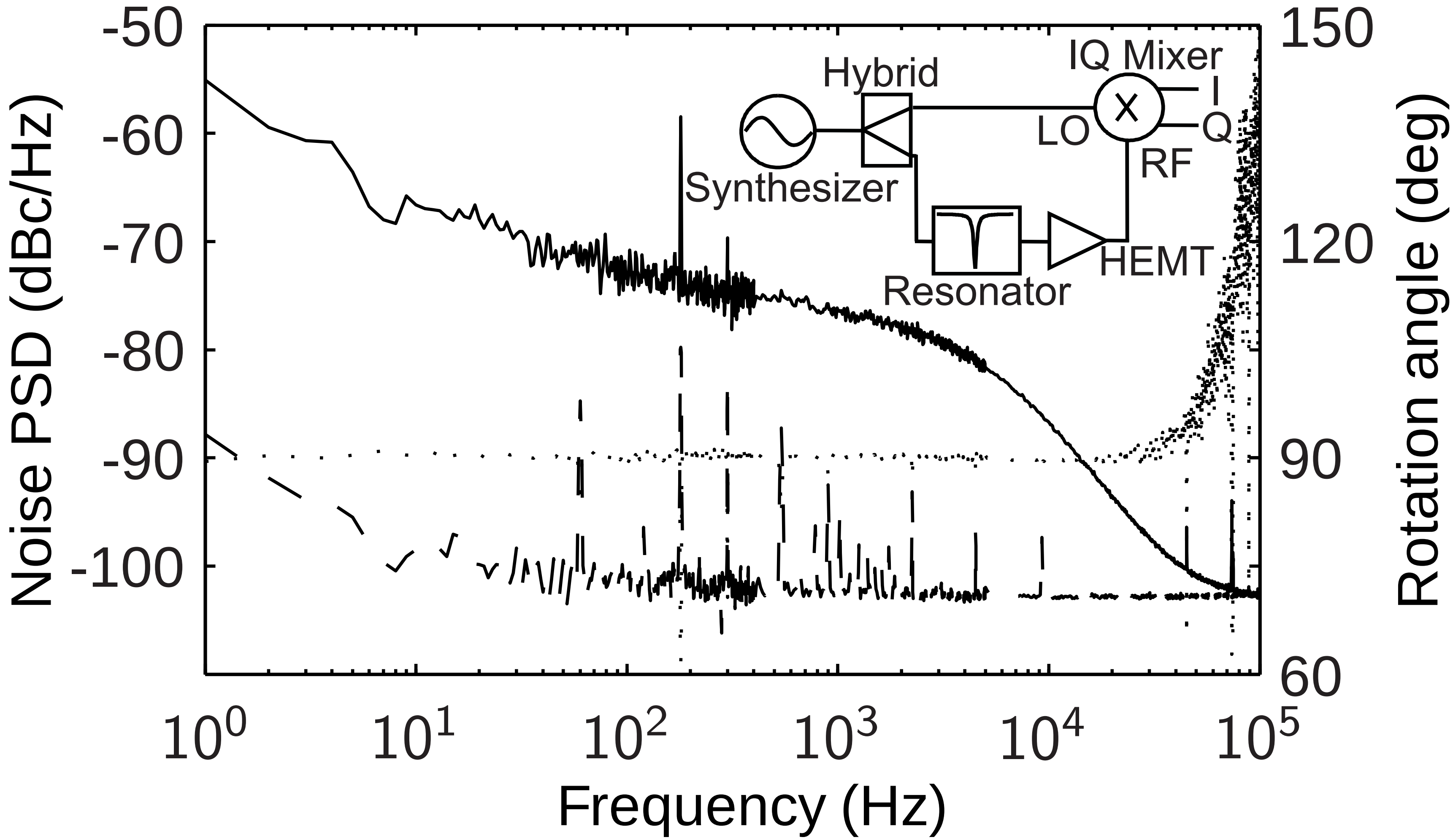
The silicon-intensive post-FFT digital downconverter is shared (*time multiplexed*) among the 256 outputs.

MKID Noise

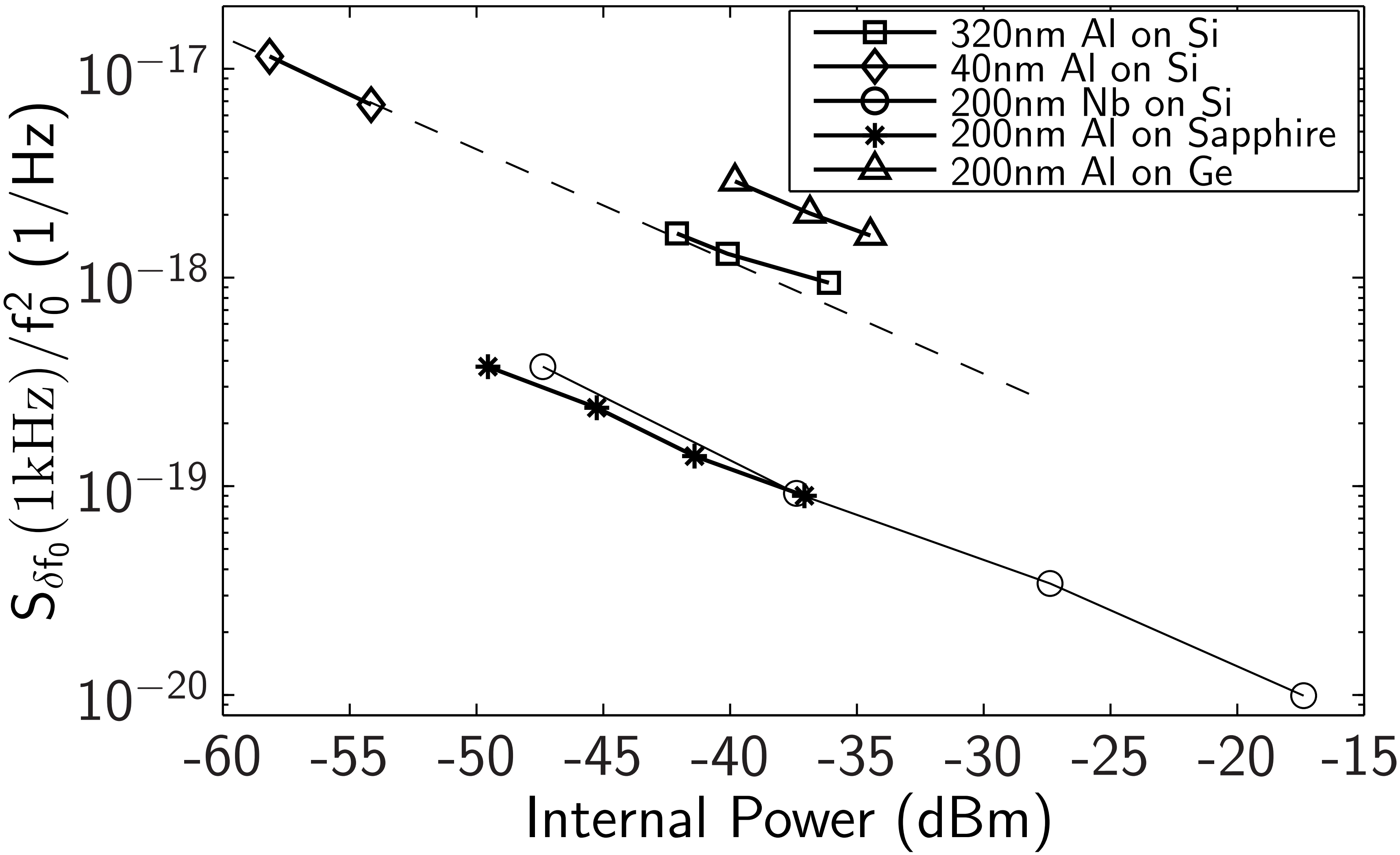


(a) (b) (c)

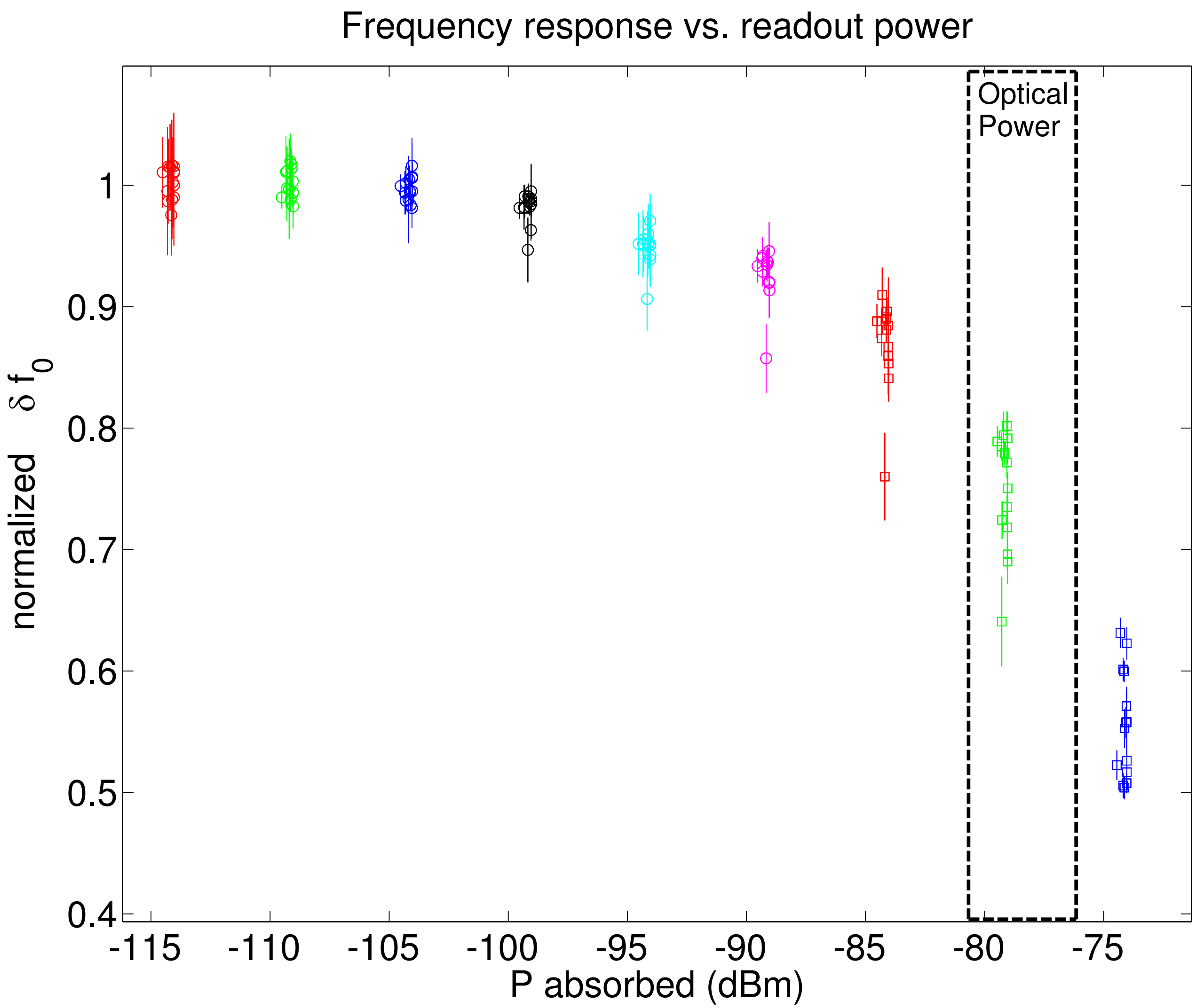
MKID Noise: frequency vs. dissipation fluctuations



MKID Noise: power scaling



MKID submm response vs. microwave readout power



Conclusion: $P_{\mu W} \approx P_{\text{submm}} \sim 10$ pW.

HEMT and ADC noise

- Best case: MKID amplitude noise due to background photon statistics rises above HEMT LNA noise.

- ADC noise should be kept below HEMT noise, $k_b T_{\mathrm{LNA}} \Delta\nu$, where $T_{\mathrm{LNA}} = 2 - 5$ K for a modern cryogenic HEMT.

- Maximum readout power: $P_{\mu\mathrm{W}}^{(\mathrm{max})} \approx P_{\mathrm{submm}} = \eta k_B T_{\mathrm{load}} \Delta f$.

- LNA noise to readout carrier ratio for $\Delta\nu = 1$ Hz is:

$$\rho_{\mathrm{LNA}} = \frac{k_B T_{\mathrm{LNA}} \Delta\nu}{P_{\mu\mathrm{W}}^{(\mathrm{max})}} = \frac{T_{\mathrm{LNA}} \Delta\nu}{\eta T_{\mathrm{load}} \Delta f} \approx 3 \times 10^{-12},$$

  or in engineering units, around -115 dBc/Hz.

- How low is the ADC noise ? Better than -115 dBc/Hz ?

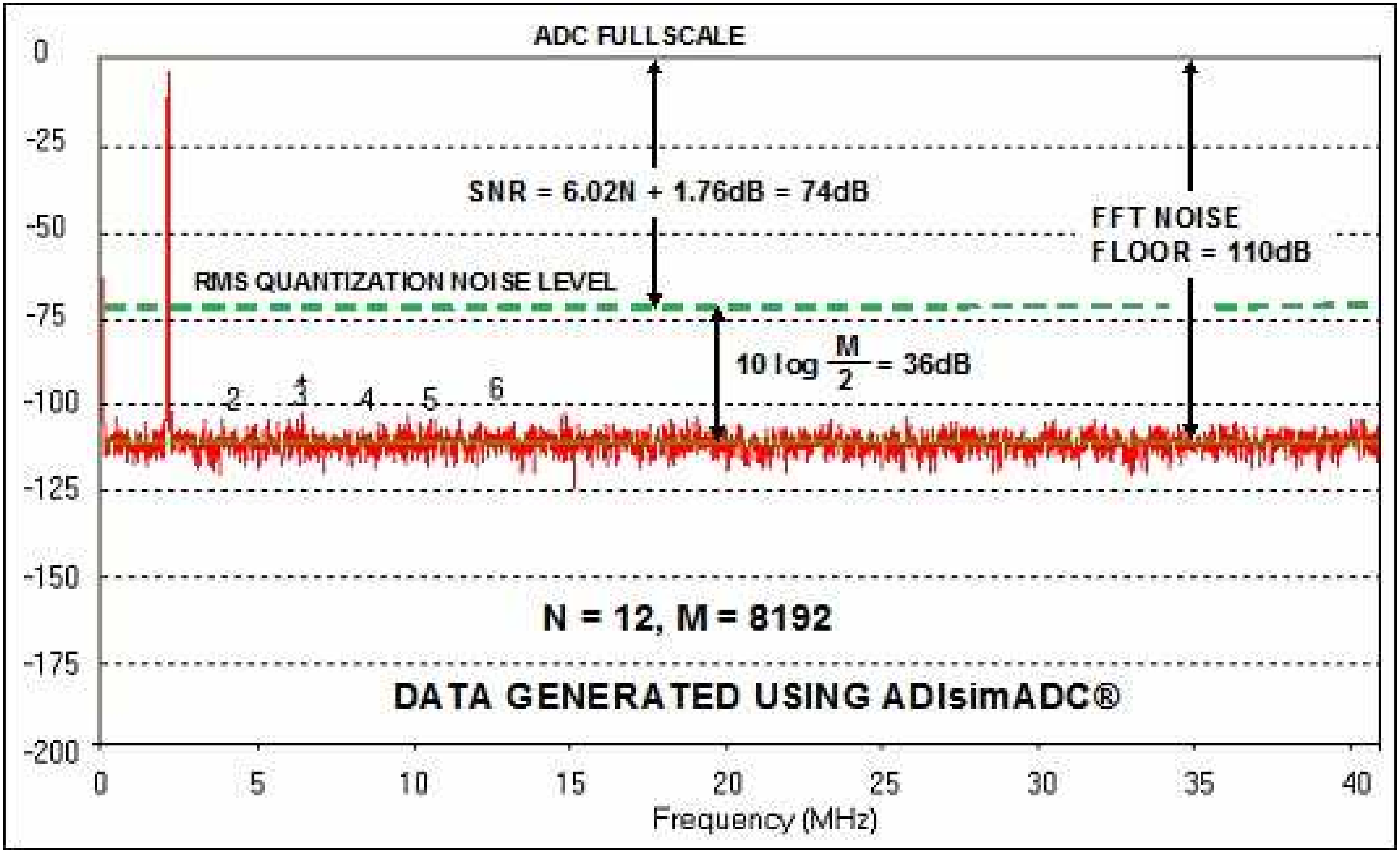
ADC quantization noise, SNR

- ADC quantization noise, uniform distribution, in LSB= 1 units:

$$\sigma^2 = \int_{-1/2}^{1/2} x^2 dx = \frac{1}{12} \ .$$

- Maximum signal amplitude is $A = 2^N/2$ (positive and negative).
- Signal power for sine wave is $P_{\text{max}} = A^2/2 = 2^{2N}/8$.
- Signal to noise ratio: SNR $= P_{\text{max}}/\sigma^2 = 2^{2N} \times 12/8 = 2^{2N} \times 3/2$.
- Decibels: SNR$= 10 \log_{10}(2^{2N} \times 3/2) = 6.02N + 1.76$ dB.
- The noise power is spread across entire Nyquist bandwidth, $\nu_S/2$.

ADC noise: definition of SNR



Note: M-point FFT spreads noise power into $M/2$ bins.

ADC dynamic range requirement

- The best noise to carrier ratio that an ADC can achieve for a 1 Hz bandwidth is given by
$$\rho_{\mathrm{ADC}}^{(\mathrm{min})} = \frac{1}{0.5\nu_S\,\mathrm{SNR}}\ .$$
This quantity is a measure of the dynamic range of the ADC.

- Frequency multiplexing of N_c carriers requires carrier power at the ADC input to be reduced to P_{max}/N_c (the carrier powers add since frequencies are incommensurate).

- For $N_c = 144/2$ channels, we need:
$$\rho_{\mathrm{ADC}}^{(\mathrm{min})} < \rho_{\mathrm{LNA}}/N_c = -115 - 10\log_{10}(72) = -134 \text{ dBc/Hz}.$$

- Equivalently, for $\nu_S = 400$ MHz,
$$\mathrm{SNR} > +134 - 10\log_{10}(200 \text{ MHz}) = 51 \text{ dB}, \mathrm{or\ ENOB} = 8.7$$

ADC dynamic range requirement, part 2

- More generally:

$$\text{SNR} \geq \frac{1}{0.5\nu_S} \frac{N_c}{\rho_{\text{LNA}}}$$

- However, resonator frequency spacing $\Delta\nu_c$ needs to be kept constant.

- Therefore:

$$\text{SNR} \geq \frac{1}{\Delta\nu_c \, \rho_{\text{LNA}}}$$

- For $\Delta\nu_c = 2.8$ MHz,

$$\text{SNR} \geq 115 - 10 \log_{10}(2.8\,\text{MHz}) = 51 \text{ dB}.$$

- SNR generally decreases with sampling rate, so the requirement above dictates the maximum usable sampling rate.

The TI ADS5474 14–bit, 400 MSPS ADC

TEXAS INSTRUMENTS
www.ti.com

ADS5474

SLAS525–JULY 2007

14-Bit, 400-MSPS Analog-to-Digital Converter

FEATURES

- 400-MSPS Sample Rate
- 14-Bit Resolution, 11.2-Bits ENOB
- 1.4-GHz Input Bandwidth
- SFDR = 80 dBc at 230 MHz and 400 MSPS
- SNR = 69.8 dBFS at 230 MHz and 400 MSPS
- 2.2 V_{PP} Differential Input Voltage
- LVDS-Compatible Outputs
- Total Power Dissipation: 2.5 W
- Power Down Mode: 50mW
- Offset Binary Output Format
- Output Data Transitions on the Rising and Falling Edges of a Half-Rate Output Clock
- On-Chip Analog Buffer, Track-and-Hold, and Reference Circuit
- TQFP-80 PowerPAD™ Package (14 mm × 14 mm footprint)
- Industrial Temperature Range: –40°C to +85°C
- Pin-Similar/Compatible with 12-, 13-, and 14-Bit Family: ADS5463 and ADS5440/ADS5444

APPLICATIONS

- Test and Measurement Instrumentation
- Software-Defined Radio
- Data Acquisition
- Power Amplifier Linearization
- Communication Instrumentation
- Radar

Note: ENOB $= 11.2 > 8.7$

SNR plot for TI ADS5474

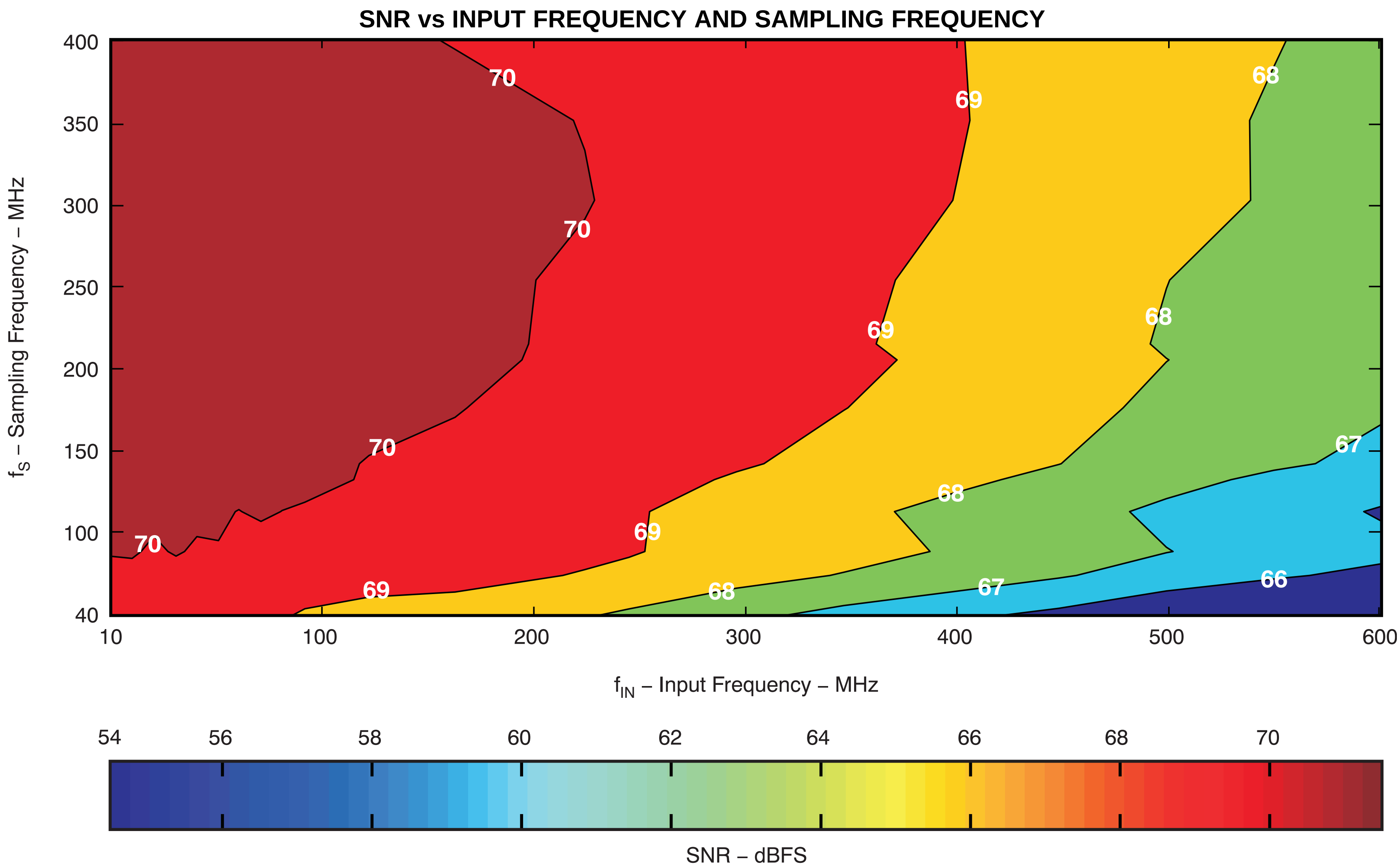
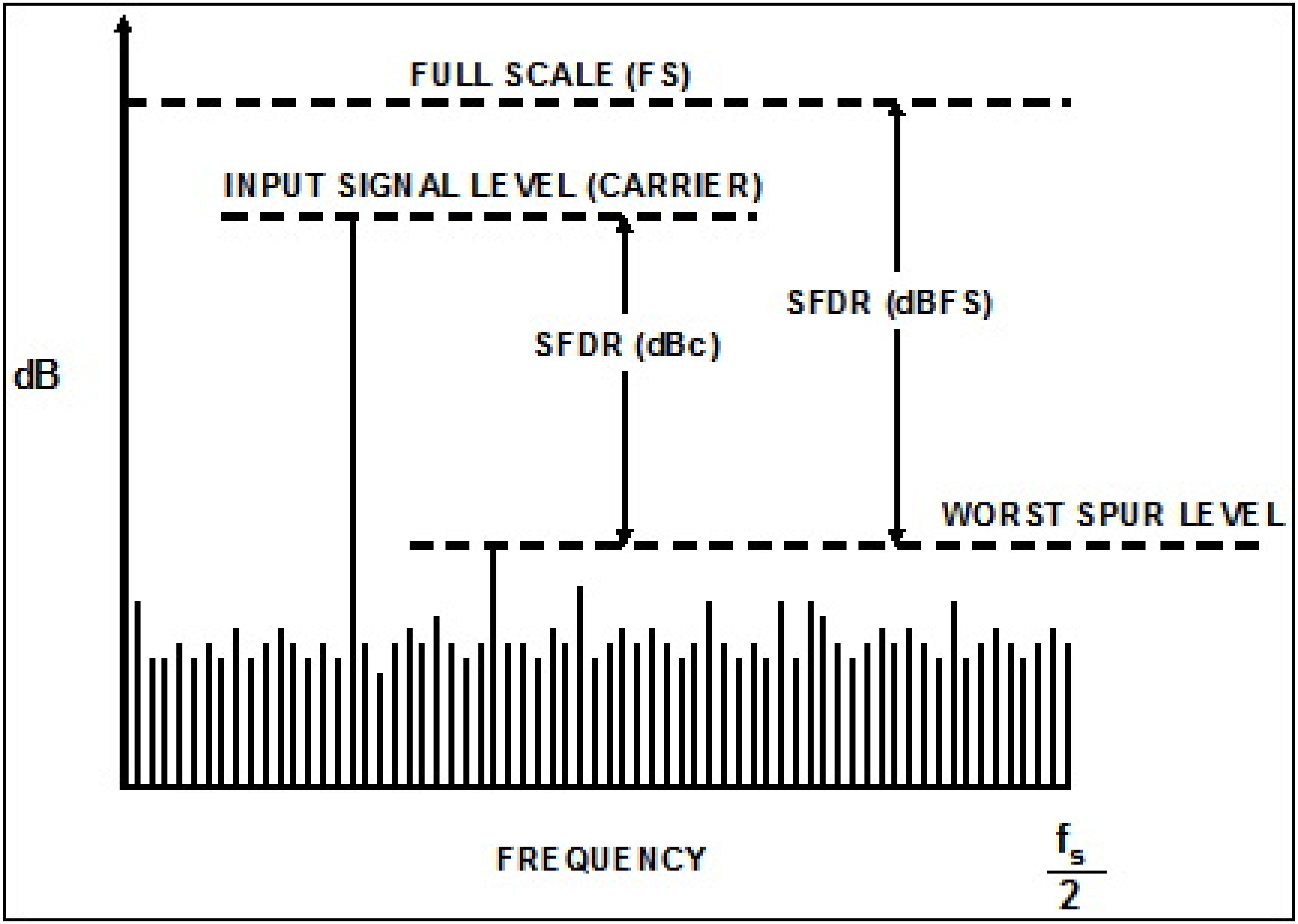
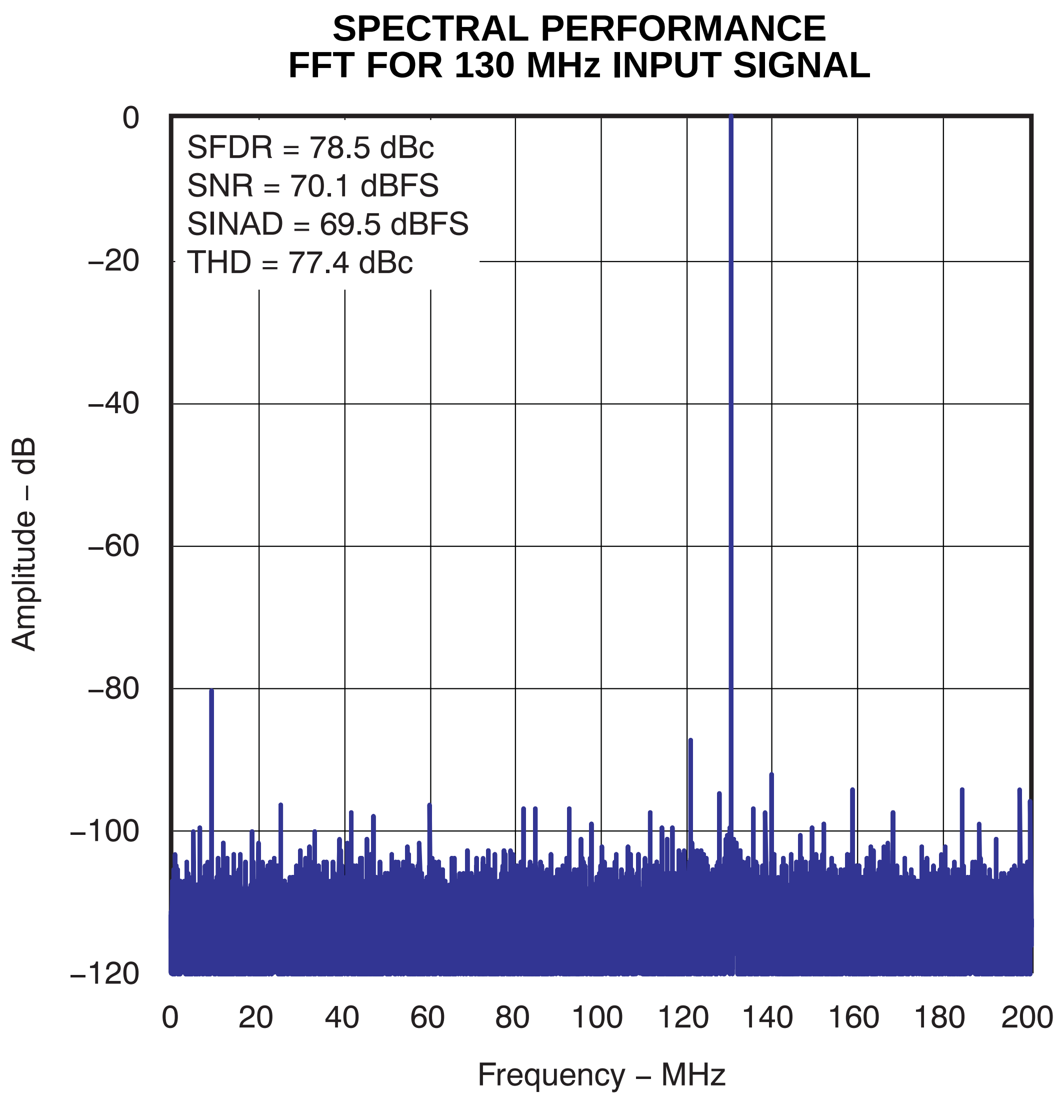


Figure 29.

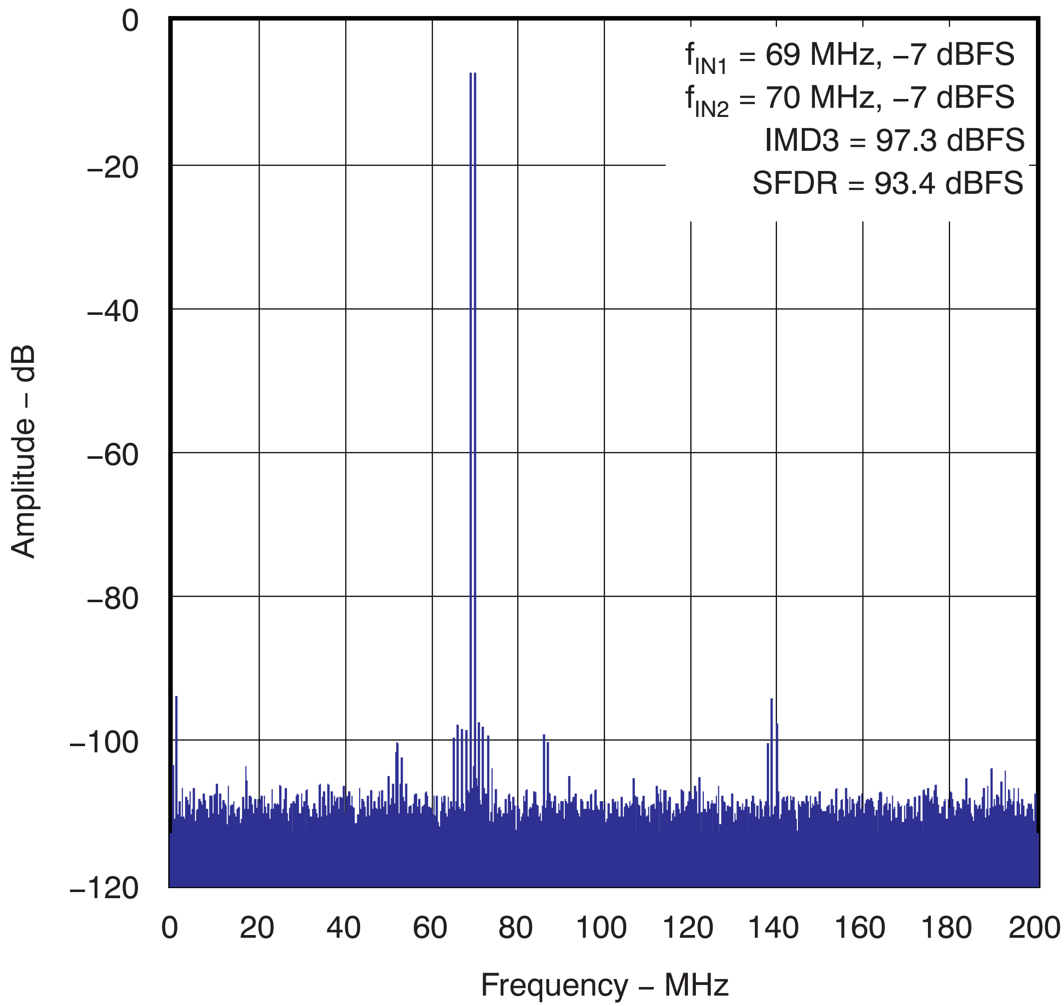
SFDR Definition



Typical spectrum for TI ADS5474



Two-tone spectrum for TI ADS5474



SFDR plot for TI ADS5474

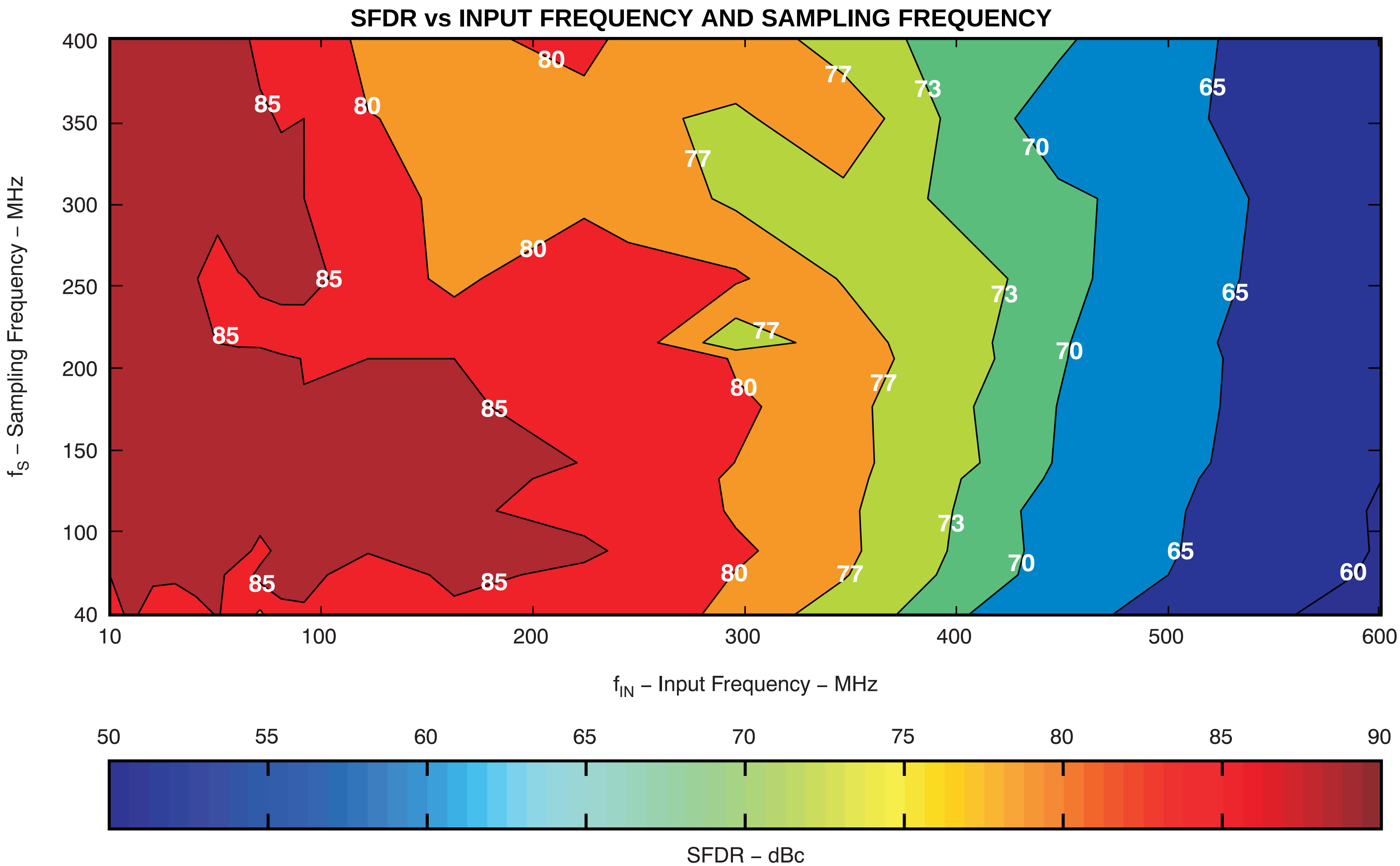


Figure 30.

Conclusions

- Digital readout for 144 channel MKID array looks highly feasible.
- Need ENOB = 8.7 bits and SNR = 51 dB, doable at 400 MSPS.
- ATMEL/e2V has a 2 GSPS, 10 bit digitizer but with SNR = 40 dB and ENOB = 6.4 bits. Not quite good enough !
- Output data rate around 100 Hz is fine.
- Hybrid FFT/DDC channelizer demonstrates required channel count.
- Spurs, harmonics, intermodulation products, etc. need to be investigated, but most likely OK. Modulation of sky signal will remove offets. "Hit probability" is low, $0.5 N_c (N_c - 1) \times 100$ Hz/400 MHz = 0.25%. Walsh function carrier modulation could be implemented.