Recommendation of NJ132L's for Pop-Up FET modules

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Summary

For the SHARC2 pop-up application (a common drain voltage follower with V_{drain} = 5V, I = 25 μA, T ~ 130 K), the InterFET NJ132L devices are suitable. Approval of the devices for HAWC is requested.

History

The NJ132L's have been used in SuZIE (Berkeley/Caltech cosmology experiment), Python (Princeton cosmology experiment) and Hertz (Chicago ISM polarization experiment) with good noise characteristics, although running at higher power than for the Pop-Up modules. They have been selected for Bolocam (Caltech cosmology experiment). The quoted noise (grounded gates) is as follows:

- SuZIE -- 2.0 nV $Hz^{-1/2}$ at 100 Hz, no current specification (W. Holzapfel, Ph.D. thesis)

- Python -- 4.0 nV Hz-1/2 (FET + preamp) at 10 Hz, < 2.4 mA (J. Ruhl, Ph.D. thesis)

- Hertz, NJ132L in transistor package (TO-72), V_{drain} = 5V, I = 600 μA, T ~ 145K, measurements by D. Dowell, 1996:

  e_n (FET + preamp) = 14 nV $Hz^{-1/2}$ at 1 Hz
  e_n (FET + preamp) = 7 nV $Hz^{-1/2}$ at 3 Hz
  e_n (FET + preamp) = 7 nV $Hz^{-1/2}$ at 5 Hz
  e_n (FET + preamp) = 7 nV $Hz^{-1/2}$ at 10 Hz

  Most (> 50%) of the noise at the specified frequencies was due to the preamp.
  No more than 2 out of 64 FETs in Hertz were replaced due to excess noise (approx. > 12 nV $Hz^{-1/2}$ at 3 Hz) -> 97% yield.

Further FET tests

Two NJ132L dies (no pre-selection) were characterized at Caltech in August 1998. For the pop-up operating conditions (V_{drain} = 5V, I = 25 μA, T ~ 130 K), the average noise of the two similar devices was:

e_n (FET + preamp) = 7.7 nV $Hz^{-1/2}$ at 4 Hz
e_n (FET + preamp) = 5.7 nV $Hz^{-1/2}$ at 10 Hz
e_n (FET + preamp) = 4.8 nV $Hz^{-1/2}$ at 40 Hz

The FET output impedance at the operating point was approximately 800 ohms. The source voltage matching was not good. (No attempt at matching was made.) The source voltages were approximately 0.7 V and 0.2 V.

9 further NJ132L dies (no pre-selection) were measured quickly at Caltech in December 1998 for a replacement package for SHARC1. The were run at V_{drain} = 5V, I = 600 µA, and T ~130 K. The average noise of 8 similar devices was:

e_n (FET + preamp) = 11 nV $Hz^{-1/2}$ at 4 Hz
e_n (FET + preamp) = 6.9 nV $Hz^{-1/2}$ at 10 Hz
e_n (FET + preamp) = 5.0 nV $Hz^{-1/2}$ at 40 Hz

The cable into the preamp was not shielded properly, so the true noise is probably lower than the measured noise. The noise of the 9th device was unacceptable: 72, 41, and 31 nV $Hz^{-1/2}$, repectively. The source voltages had a mean of 0.29 V and a standard deviation of 0.12 V.

Handling and wire bonding of the NJ132L dies was straightforward and was done at Caltech by D. Dowell and D. Miller.

Proposal

The NJ132L dies will be used for the Pop-Up FET modules. The procedure for the construction of the modules will allow for a preliminary noise test with shorted gates at ~130 K and a single attempt to improve the module by replacing noisy devices. The noise specifications for the test conditions of T ~ 130K, V_{drain} = 5V, I = 25 µA are to be:

90% of devices -- e_n < 12 nV $Hz^{-1/2}$ at 4Hz
< 8 nV $Hz^{-1/2}$ at $f \geq 10$ Hz
95% of devices -- e_n < 20 nV $Hz^{-1/2}$ at 4Hz
< 15 nV $Hz^{-1/2}$ at $f \geq 10$ Hz

The yield specification covers FET performance and wire bonding but does not cover assembly structures (such as silicon microbridges).

For the SHARC2 modules only, the source voltage at the operating conditions will be matched. The target is to match the source voltage for groups of 32 FETs reading out a detector row to 50 mV.

Limitations

The NJ132L devices have a typical input capacitance of 15 pF. For a 20 MΩ bolometer impedance, this creates an electrical cutoff frequency at ~530 Hz (3 dB point). (Parasitic capacitances from the fanout structure may be of the same order.)

The temperature of the devices must be maintained above 100 K. Between 75 and 95 K, the FETs are extremely noisy. The performance at 75 K does not appear to be as good as at > 100 K.

The devices are known to have large gate current noise (gate leakage) for overly large drain voltages; 12 V is too much. This behavior is common to FETs. A drain voltage of 5 V is sufficient to achieve saturation and will result in a lower power disspiation.