Constructing Your Power Supply- Layout Considerations

Robert Kollman

ABSTRACT

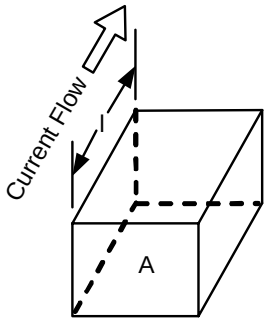
Laying out a power supply design is crucial for its proper operation; there are many issues to consider when translating a schematic into a physical product. This topic addresses methods to keep circuit parasitic components from degrading the operation of your designs. Techniques to minimize the impact of parasitic inductance and capacitance of filter components and printed wire board (PWB) traces is discussed, together with a description of the impact that PWB trace resistance can have on power supply regulation and current capacity. A general overview of thermal design is also included as well as sample temperature rise calculations in a natural and forced-air environment. Finally, some practical examples of power stage and control device layouts are reviewed.

I. INTRODUCTION

There have been numerous articles written on this subject, including Topic 2 of SEM-1500, because of its importance in ensuring a successful design. This article gathers useful guidelines and calculations to enable the neophyte as well as the experienced engineer to understand issues in physically realizing the electrical schematic. The paper covers parasitic components that can create havoc with the design with degradation in efficiency, regulation, high ripple, or just chaotic power supply operation. Included is a short section on grounding and if a more detailed discussion is desired, the reader is referred to "*Noise Reduction Techniques in Electronic Systems*" by Henry Ott [1]. One of the common problems power supply designers are facing is that their power supply is part of a motherboard and the system designers are expecting the power supply construction to be similar to the rest of the motherboard. One of these expectations may be that the power supply employs no heatsink. This means that the engineer needs to understand cooling solely provided by the motherboard surface area. Also included is a large section that discusses practical conduction, convection and radiation heat transfer. Finally, the last section provides some real world layout examples of what to do in the power stage and control section of the power supply.

II. DC PARASITICS (RESISTANCE)

In high current power supplies, resistance of components is always an issue as it degrades efficiency, can create cooling problems, and may also impact regulation. Even with it being a problem, the resistance of the PWB traces is overlooked and adds to the issue. Resistance of a conductor is easily calculated from its resistivity and physical dimensions as shown in Fig. 1. The equation states the longer the path, the more the resistance; or the greater the cross section, the lower the resistance. So a short, large cross section conductor would be desirable to control interconnect resistance. Fig. 1 also presents the resistivity of some common materials that may be found in power supply construction. One interesting point is that plated copper is much more resistive than pure copper. This is important to understand in power supplies because plating is used to form vias to make interconnect in PWBs and also plating is applied to the surface of the PWBs to increase the copper thickness. Many times surface layers are "1 plate 1" meaning the starting copper material is 1-oz (or 1.4 mils or 0.4 mm) thick and an additional 1 oz of copper is plated on to form vias and increase the surface thickness. The surface resistance reduction will only be about 25% of what one may expect. Another interesting point is that solder materials such as tin-lead or other plating materials such as tin are not very good conductors.



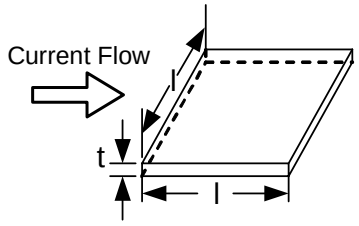
$$R = \frac{\rho l}{A}$$

Fig. 1. Sample resistance calculation and common resistivities.

TABLE 1. SAMPLE RESISTIVITIES (25ºC)

Material	μΩ-cm	μΩ-in
Copper	1.70	0.67
Copper (Plated)	6.0	2.36
Gold	2.2	0.87
Lead	22.0	8.66
Silver	1.5	0.59
Silver (Plated)	1.8	0.71
Tin -Lead	15	5.91
Tin (Plated)	11	4.33

A simple way to estimate the resistance of PWB traces is presented in Fig. 2. The first step is to calculate the resistance across a square of conductor. From the resistance formula, if the conductor width and length are equal, they cancel out and the square resistance is dependent only on thickness and resistivity. Table 1 presents sample calculations for a number of common trace thicknesses and temperature. Note that at 100ºC resistance increases by 30%. The resistance of copper varies linearly with temperature and doubles from 25ºC to 279ºC. Once the square resistance is calculated, the designer can then estimate the number of squares in the PWB trace and multiply by the square resistance to calculate total resistance. Remembering that a square of 1-oz copper has about 0.5 mΩ of resistance is much easier than remembering the resistivity of copper and measuring trace widths and lengths.



$$R = \frac{\rho l}{(tl)}$$

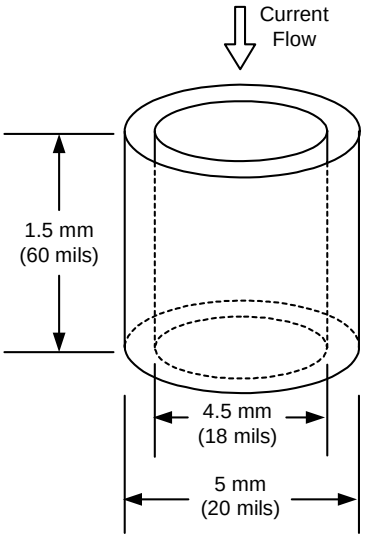
$$R = \frac{\rho}{t}$$

Fig. 2. A PWB trace square has constant resistance.

TABLE 2. PWB TRACE RESISTANCE

Copper Weight (Oz.)	Thickness (mm/mils)	mΩ per Square (25ºC)	mΩ per Square (100ºC)
1/2	0.02/0.7	1.0	1.3
1	0.04/1.4	0.5	0.6
2	0.07/2.8	0.2	0.3

An often overlooked current path is through vias from the front to back of the board and they can have significant resistance. Fig. 3 presents a sample calculation for a via through a 1.5-mm (0.060 in) thick PWB. A plated wall thickness of 0.03 mm (1 mil) and a plating resistivity of 6 μΩ/cm (2.4 μΩ/in) are assumed and a resistance of 2.4 mΩ was calculated. While this may not sound significant, if this were the only path for a 10-A output, it would result in ¼ W of dissipation and in a voltage drop of 24 mV. For a 1.2-V output, this could be 2% load regulation degradation. A typical rule of thumb limits the current through vias to between 1 A and 3 A. Not only should the output path for the power supply be scrutinized, but high-current AC paths around switching devices need to be considered. Note that there can be voltage drops from the point of regulation to the load and a good design will place the point of regulation as close to the load as possible.



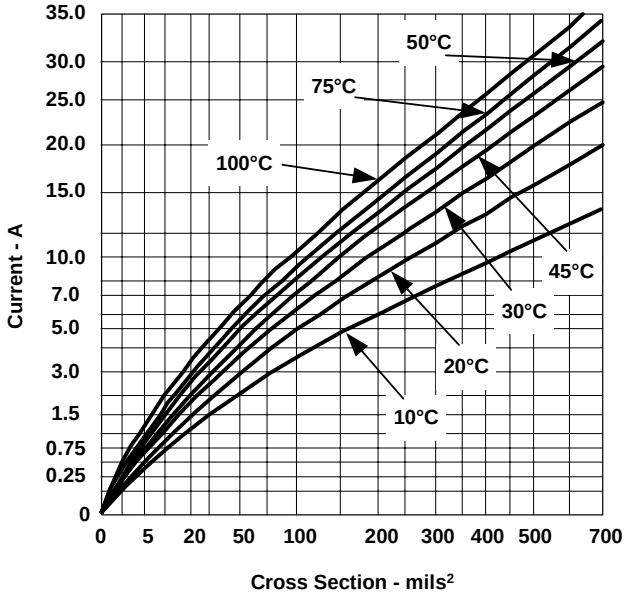
$$R = \frac{\rho l}{A}$$

$$R = \frac{\rho l}{\pi(r_o^{\,2} - r_i^{\,2})}$$

$$R = \frac{2.36\times10^{-6}\times0.06}{\pi(0.01^2 - 0.009^2)} = 2.4\ m\Omega$$

Fig. 3. Vias have resistance too!

A second consideration in sizing PWB traces, in addition to voltage drop, is the temperature rise of the conductor. As discussed with the vias, even a few milliohms of resistance can generate significant power and consequently significant temperature rise. The Institute for Interconnecting and Packaging of Electronic Circuits (IPC) has published Fig. 4 in IPC-2221A to be used as a guideline in determining appropriate conductor widths for a given temperature rise. This data was created in the early 1950's and is very conservative. IPC recognizes that this data is conservative and has a task underway to update and add to this information under IPC 1-10b Current Carrying Capacity Task Group and expects to have review information available during 2003. As a example of the use of the chart, consider a 0.1-inch wide, 1-ounce trace. For 10ºC rise, the conductor current carrying capacity is 4 A, and for 45ºC rise it would be 9 A. These curves show extremes of how much current a trace can carry, but do not comprehend voltage drop. Consider a 1-ounce, 1-inch long by 0.1-inch wide trace. It is 10 squares long and with 0.5 mΩ per square, it has a resistance of 5 mΩ. So 10ºC rise equates to a 20-mV drop and 45ºC rise equates to a 45-mV drop. Usually these types of drops are excessive, particularly in 1-V power supplies, so if the conductor is sized properly for good regulation, temperature rise should not be a problem.



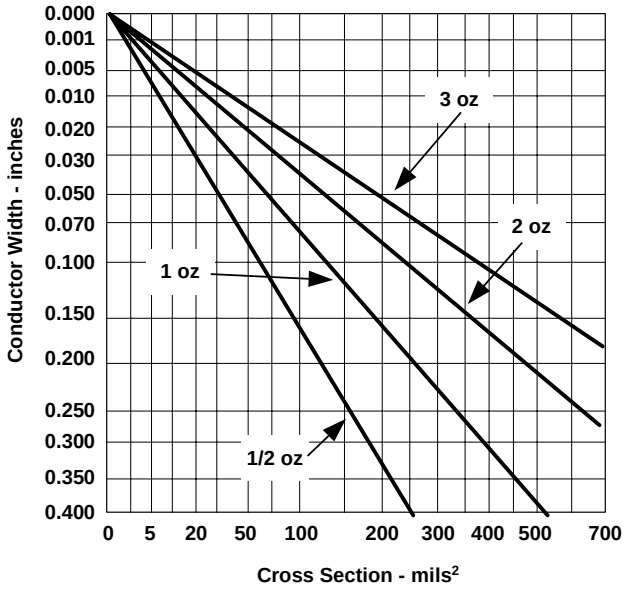


Fig. 4. IPC's conservative current derating guideline.

Some of the printed circuit traces may have large AC current components. Depending upon skin and proximity effects, AC resistance could conceivably be much greater than DC resistance, with high AC losses. Current distribution in these traces is determined by their physical size and proximity of return paths for the current. As an extreme example, a current in a trace far away from the return path tends to gather toward the edges of the conductor at a thickness of one skin depth. So even with a very wide conductor, high-frequency currents may use only a small portion. With a trace over a return path, the current pulls toward the opposing surfaces. If the trace is thicker than one skin depth, AC current flows only on the inner surface of the trace facing the opposing conductor – the outer surface carries little current. However, skin depth in copper is 0.25 mm at 100 kHz, and varies inversely with the square root of the frequency. Thus, even at 1 MHz, AC current penetrates through the entire 0.07-mm thickness of a 2-oz. copper trace. Therefore, in most applications, the AC resistance of a printed circuit trace is not significantly greater than its DC resistance.

III. AC Parasitics

Just as PWB traces add unseen resistors to schematics, they can also add inductors, capacitors, and transformers. Fig. 5 illustrates that parasitics can destroy the performance of a capacitor even before it is mounted. The impedance of four different styles of capacitors was measured. At low frequencies, they all exhibit the expected diminishing impedance as the frequency is increased. However, they each reach a frequency where the impedance no longer decreases, but instead, starts to increase. This increasing impedance is caused by the equivalent series inductance (ESL) of the part which to a first order can be estimated by the physical dimension of the part and the rule of thumb for the inductance of a conductor of 6 nH/cm (or 15 nH/in). For instance, the 10-µF ceramic capacitor is about 0.5 mm (or 0.12 in) long, and would have an estimated inductance of 0.5 mm x 6 nH/mm = 3 nH. The right side of the chart is marked with the impedance of 1-nH and 5-nH inductors and the correlation is good for the ceramic and the larger electrolytic capacitors. Also, note that it doesn't take much printed circuit trace inductance (or length) to further degrade the capacitors.

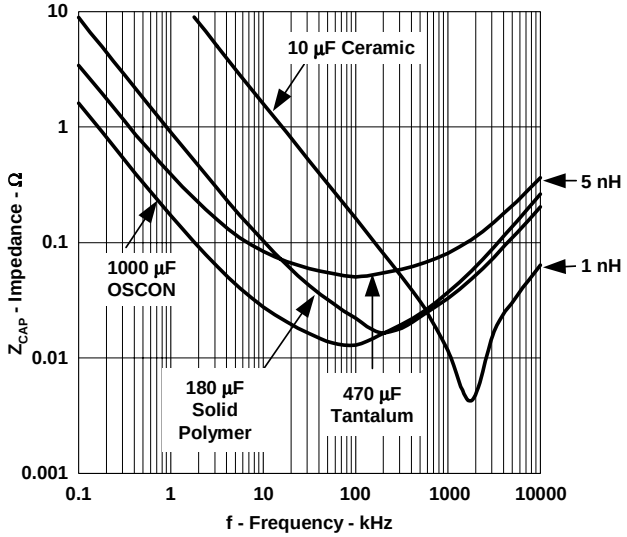
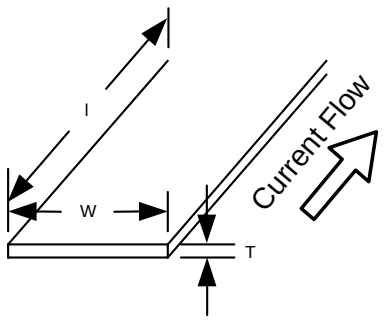


Fig. 5. Before capacitors are even mounted, parasitic inductance is evident.

Fig. 6 provides a precise inductance calculation. This is for a PWB trace in free space and is taken from page 35 of Grover [6]. An important note on all inductance formulas is that many are empirical, and it is very important to understand the allowable extremes of the variables. This particular one is good for large extremes of variables. It calculates the rule of thumb 6 nH/mm (or 15 nH/in). It is interesting to note that due to the natural log relationship, large changes in conductor width have minimal impact on inductance. With a 50-to-1 increase in conductor width, inductance is only decreased by a factor of four. This means it is a real problem trying to drive down the inductance of an isolated trace!



$$L = 2l\left(\ln(\frac{l}{(T+W)}\right) = \frac{1}{2}) \; nH(cm)$$

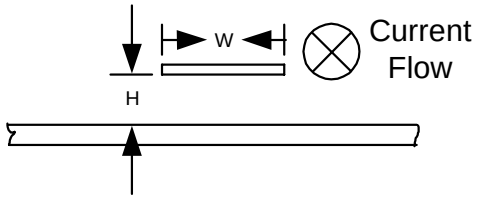
$$L = 5l\left(\ln(\frac{L}{(T+W)}\right) + \frac{1}{2}) \; nH(in)$$

Fig. 6. Self-inductance equation aligns with 6 nH/cm (15 nH/in) rule of thumb.

TABLE 3. INCREASING CONDUCTOR WIDTH REDUCES ITS INDUCTANCE SLIGHTLY

W (mm/in)	T(mm/in)	Inductance (nH/cm or nH/in)
0.25/0.01	0.07/0.0028	10/24
2.5/0.1	0.07/0.0028	6/14
12.5/0.5	0.07/0.0028	2/6

Fig. 7 provides an expression to calculate inductance of a trace over a ground plane from Reference [7]. This is a transmission line calculation and it is only good for large ratios of conductor trace widths to separation from the ground plane. One key point in the formula is that the inductance is proportional to spacing and inversely proportion to conductor width. This means that there is much more control of inductance as compared to an isolated conductor. A second point is that the inductance is proportional to the area enclosed by the conductors. To minimize inductance, one needs to minimize the area enclosed by the current flow. This is generally the case, even in the absence of a ground plane. Fig. 7 also provides a couple of sample calculations. The first is representative of a trace in a multi-layer board over an adjacent ground plane. Note when compared to Fig. 6, the inductance has been reduced by a factor of thirty. It could be further reduced by widening the conductor. The second example inductance is that of a typical two sided board, one side ground plane and the second the conductor. Note that even in this case, the ground plane provides a 5-to-1 reduction in interconnect inductance.



$$L = \frac{2Hl}{W} \text{ nH/cm}$$

$$L = \frac{5Hl}{W} \text{ nH/in}$$

Fig. 7. Trace over ground plane significantly reduces inductance.

TABLE 4. CONDUCTOR OVER PLANE DRAMATICALLY REDUCES INDUCTANCE

MetricC			English		
H (cm)	W (cm)	Inductance (nH/cm)	H (in)	W (in)	Inductance (nH/in)
0.25	0.25	0.2	0.01	0.1	0.5
0.15	2.5	1.2	0.06	0.1	3.0

It should be noted that the effectiveness of the ground plane depends upon it being significantly wider than the trace above it. For example, if the ground plane were the same width as the trace above it in Fig. 7, the resulting symmetrical conductor pair has a total inductance per unit length slightly greater than the value calculated by the formula of Fig. 7. However, this total inductance value is distributed so that one half appears in series with each conductor. Thus, the lower conductor is no longer an effective ground plane. When the lower conductor is made significantly wider, the asymmetrical structure causes almost all of the total inductance to appear in series with the smaller conductor, thereby minimizing the impedance in series with the wider ground plane.

For capacitors to be effective, whether they are bypass or output capacitors, they need to be connected with minimal lead inductance. As the first step of the layout process, the designer should draw the schematic so the layout person knows the critical routes. The second step is the power supply designer should either plan the connections or review them. The designer should use minimum lengths on high di/dt paths; use ground planes where possible, bring current paths across capacitor terminals, and minimize bypass loop area. If a multilayer PWB is used, a ground plane is a very good idea and it should be as close to the surface of the board as possible to further minimize bypass loop area.

The designer should also consider paralleling different capacitor types for reduced impedance across the frequency band. Fig. 8 provides a good example of the advantage of this approach. It shows three impedance curves versus frequency, the first is an aluminum electrolytic capacitor, the second is a ceramic and the third is the parallel combination of the two. The electrolytic capacitor has low impedance at low frequency, but it quickly runs into its equivalent series resistance (ESR) and its impedance does not decline any further. The ceramic capacitor has a relatively high impedance at low frequencies, but since it has little ESR, its impedance is less than the ESR of the electrolytic. By paralleling the two capacitors, one can obtain low impedance across a wide frequency band. A side benefit is that the ESR of the electrolytic capacitor can damp circuit resonances. Note that the impedance does start to increase at the higher frequencies due to the ESL of the ceramic capacitor. One could consider paralleling different ceramic capacitors values to reduce impedance in the 2-MHz to 20-MHz frequency range (0.1 μF and 0.01 μF). However, this reduction will only be possible if the inductance of the smaller value capacitors is less than the large one and, in general, this means that the higher frequency capacitors need to be physically smaller.

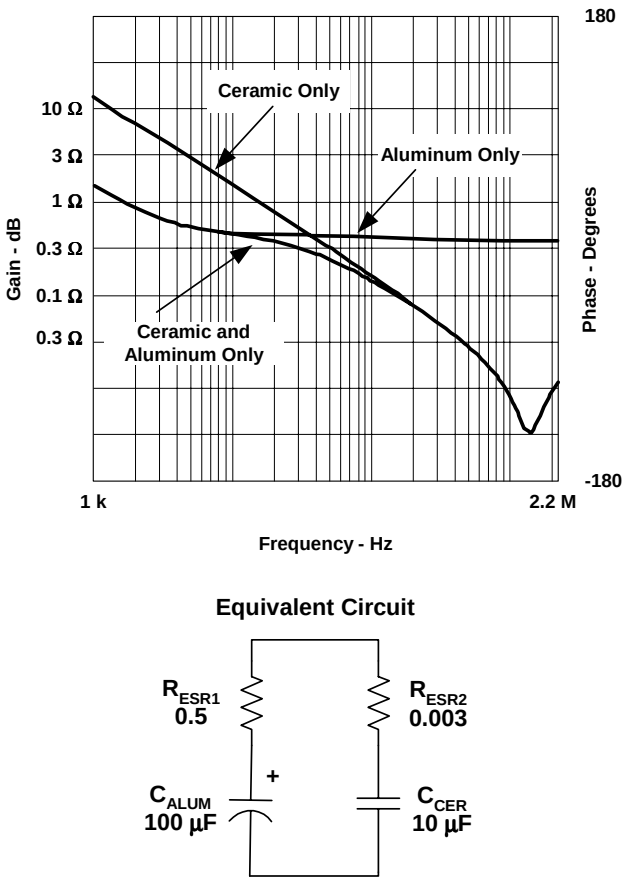


Fig. 8. Paralleled capacitors minimize impedance over frequency.

Fig. 9 presents the impedance of a common mode inductor versus frequency. At low frequency, the impedance rises as expected but at high frequency, the inductor impedance takes on a capacitive response. This is called *distributed capacitance* and is a result of winding to winding capacitance. This is an extreme example but any inductor has a similar response. It may not turn capacitive at as low of a frequency but typical distributed capacitances are in the 10-pF to 100-pF range. Just as in the case of capacitors, one can further degrade an inductor's characteristic by mounting it on a PWB.

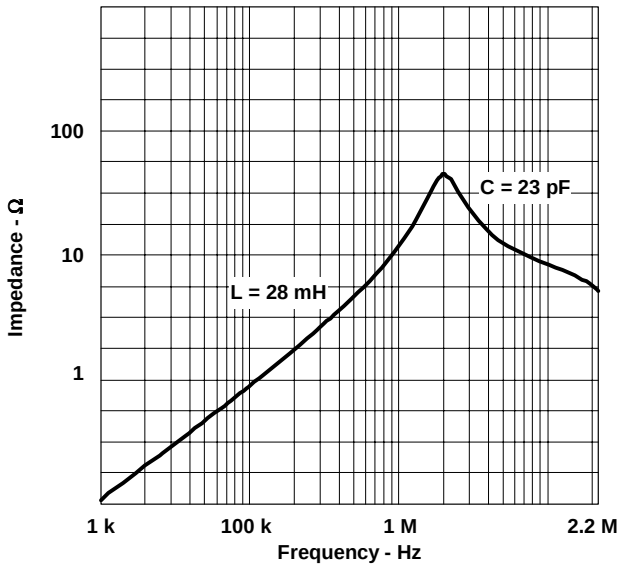


Fig. 9. At high frequencies, inductors turn into capacitors.

Fig. 10 provides a formula to calculate the capacitance from layer to layer in a PWB. The capacitance is related to the permittivity, relative permittivity, area, and thickness. Permittivity is a constant equal to $1/36\pi\times10^{-9}$ F/m whereas relative permittivity is material related. For typical PWB material, relative permittivity is about 5 F/m. The only real variables the designer has at his control is area and spacing. For low capacitance between conductors, the area should be minimized and spacing should be maximized. It can be seen from the sample calculation that 0.25 mm (10-mil) conductors crossing each other in a multi-layer board have a minimal amount of capacitance.

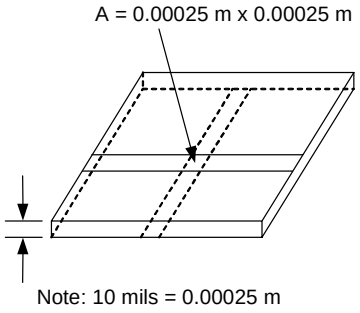


Fig. 10. Sample area to visualize capacitance calculation.

$$C = \frac{\varepsilon_R \times \varepsilon_O \times A}{t}$$

$$C = 5\left(\frac{10^{-9}}{36\pi}\right)\left(\frac{0.00025^2}{0.00025}\right)$$

$$C = 0.01\ pF$$

Crossing traces are generally not an issue due to the small capacitance. Capacitance coupling issues usually involve planes, a number of component pads or parallel conductors. For instance, Fig. 11 shows how plane capacitances can further degrade a common mode inductor. In this example, the ground plane is continuous under the inductor and there are large planes connecting the power to the inductor. This creates a significant amount of capacitance from input to ground and then to output, and adds appreciably to the distributed capacitance of the common mode inductor. To properly connect this inductor, the ground plane should not extend past the inductor, and the area connecting the leads should be minimized to avoid induced currents.

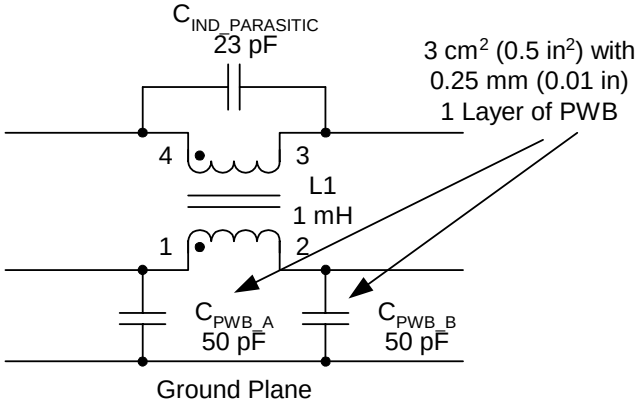


Fig. 11. Ground plane capacitance shorts common mode inductor.

The most serious parasitic capacitance issue usually involves connecting the feedback (FB) voltage and compensation of the error amplifier. This is due to the fact that it involves a high-impedance node, a lot of gain in the error amplifier and a large number of components connected to this node. Fig. 12 shows this trouble spot in a typical controller and one of the more likely coupling nodes. The connection between Q1 and D1 has very high slew rates in the order of 0.1 V to 1 V per ns and can create 1 mA of current with only 1 pF of parasitic capacitance. Typically, the impedance on the feedback and compensation nodes are on the order of 1 kΩ to 10 kΩ so this current can create significant voltage perturbations on the error amplifier input. This is usually manifested as erratic gate drives or a perceived oscillation as the power supply tries to correct for the error injected from the noise source. The most successful designs recognize this fact and draw the schematic so that the compensation components are shown in the vicinity of the error amplifier to imply a recommended routing. Then the power supply designer needs to make sure that the components are compactly placed near the error amplifier and that the traces that connect them are short. Also, the designer needs to make sure that there is not a high dV/dt trace in the vicinity of these components; this includes the switch node and gate drive signal. Finally, there is a preferred connection for the resistors and capacitors in the compensation circuit as shown in Fig. 12. It is best to connect the resistors to the FB pin because they can provide a little attenuation of an injected signal. For instance, if R9 and C7 were reversed, and a high frequency signal was applied to their common node, it would also show up on the FB pin with little attenuation. In the proper connection, R9 working against the other resistors in the compensation circuit and the input impedance of the error amplifier will provide some attenuation and a little less noisy power supply.

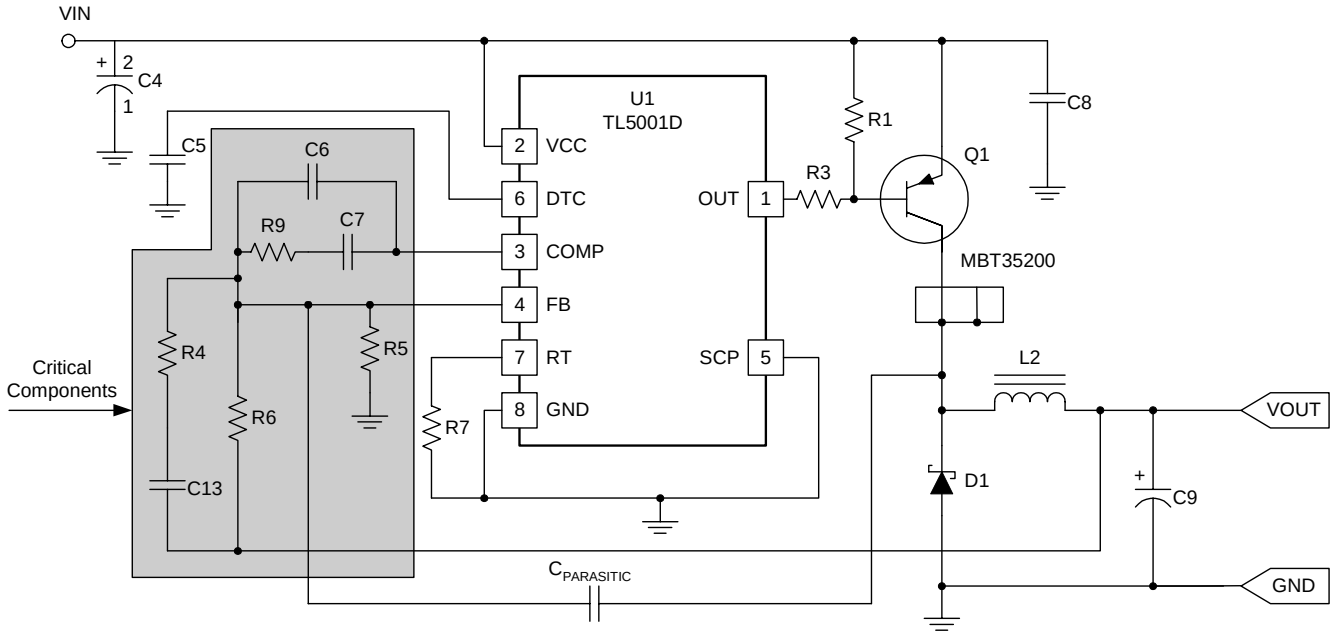


Fig. 12. FB and comp connections are the most critical route in the power supply.

Fig. 13 illustrates magnetic coupling between circuits. In this case, it is between two toroidal inductors. Each inductor represents a single loop of wire with a diameter about equal to the diameter of the inductor. Current flowing in one induces a current flow in the second. Normally, this is not an issue if these are both power components in a topology like SEPIC. However, it can become quite an issue if these are filter inductors. In a filter, it may be desirable to have 100 dB of current reduction between the two inductors and it would not be physically realizable with this layout. To improve the situation, the inductors should be oriented such that flux generated in one can not link into the second one. Shields or different core geometries are also alternative solutions. Similar situations can also occur in poorly constructed power stages. If care is not exercised to minimize the inductance of the power stage and input capacitor connections, single turn inductors with large loop areas can be created. They generate a magnetic field that couples into other loops like toroid inductors and EMI measuring devices.

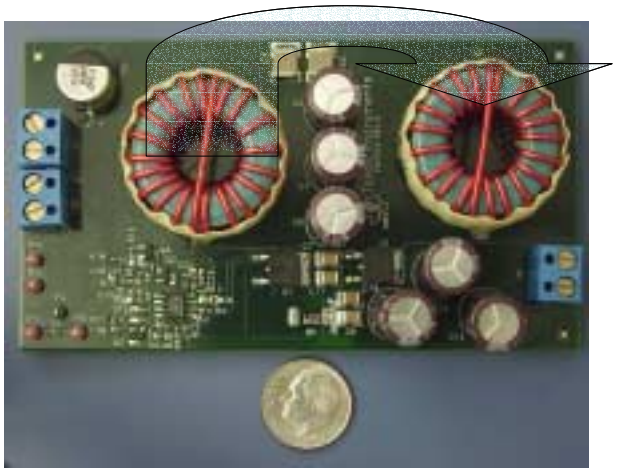


Fig. 13. Coupling between inductors can degrade filter response.

In summary, the layout of the power supply is crucial to maintaining the high frequency characteristics of the power components, thus providing a satisfactory design. Unintended inductance can ruin the filtering effects of capacitors and is especially important in low impedance circuits such as filters, power switching, and timing. To minimize inductance, use ground planes and wide conductors and strive to minimize the loop area of all high di/dt circuits. Unintended capacitance can also ruin the high-frequency performance of inductors and is especially important in high-impedance circuits such as filters and amplifiers. To minimize capacitive effects, use careful layout techniques and also shielding. Pay particular attention to error amplifier inputs and their physical relationship to high dV/dt traces on the board. A ground between a noisy circuit and a sensitive circuit can help divert parasitic currents; this is especially true if multilayer PWBs are used. In this case, power connections can be made on one side of the ground plane and low level connections can be made on the other. The final coupling mechanism is magnetic which is created by high di/dt currents flowing through circuit loops. These effects are best minimized by minimizing loop areas and by providing some shielding with ground planes. Also, watch out for emissions from devices such as toroid inductors as they can couple into other parts of the circuits. If multiple toroids are involved in a filter design, orient them at right angles (ie; horizontal and vertical) so they can not couple.

IV. GROUNDS AND GROUNDING

As with layout, grounding is one of those things that must be done correctly for a functioning system. It is very important to start a system design with a plan for grounding in the form of a system ground chart. This chart should contain the various subsystems and a plan for connecting their various grounds together. This paper introduces concepts and makes recommendations for handling the ground within the power supply portion of the system. For a thorough discussion on grounding, refer to [1].

The reason grounding is such an important topic is that there is current flow between the various elements of the system and if there is an impedance (and there always is), a voltage drop is generated. This voltage drop can degrade system performance by reduced noise tolerance for digital systems, or voltage offsets in analog systems leading to sensing errors. The currents between the subsystems can take a number of forms, it can simply be DC current as power is distributed throughout the systems, it can be common mode current that is generated by power supply, it can be lower frequency AC current either from the mains or motors or solenoids, or it can be radio frequency created by transmitters. Whatever the source, the ground plan should comprehend the current's nature and plan for a low impedance return path.

Fig. 14 presents two common ground schemes for a system. In the series connection, the subsystems are daisy chained together to provide the current return path. In this plan, ideally, box 1 would represent the highest current draw followed by box 2 and then box 3. In this manner, the highest current draw and presumably highest voltage drop would be eliminated from common current paths. This is the simplest grounding scheme but has the drawback that the additive effect of the ground currents from each subsystem generates differential voltages between the subsystems. Also, the inductance of these connections can be quite high. The parallel connection helps to mitigate some of these issues. In this scheme, the subsystems are connected to single point ground in a star arrangement. Current flow in these ground connections are only from the subsystem itself. This reduces the current flow in the ground connections and thereby reduces some of the differential voltage differences between the subsystems. This is a more complicated wiring scheme and has the drawback that the wiring can be high impedance at high frequency.

The ideal case for a ground system is presented in Fig. 15. In this approach, the various subsystems are interconnected through a very low-impedance ground plane. The ground plane is made significantly thick enough to eliminate differential low-frequency voltages and interconnect inductance is minimized much in the same way inductance of a conductor is minimized when it is put over a ground plane. This is the preferred approach for a power supply layout whether it is a two-sided PWB or multilayer.

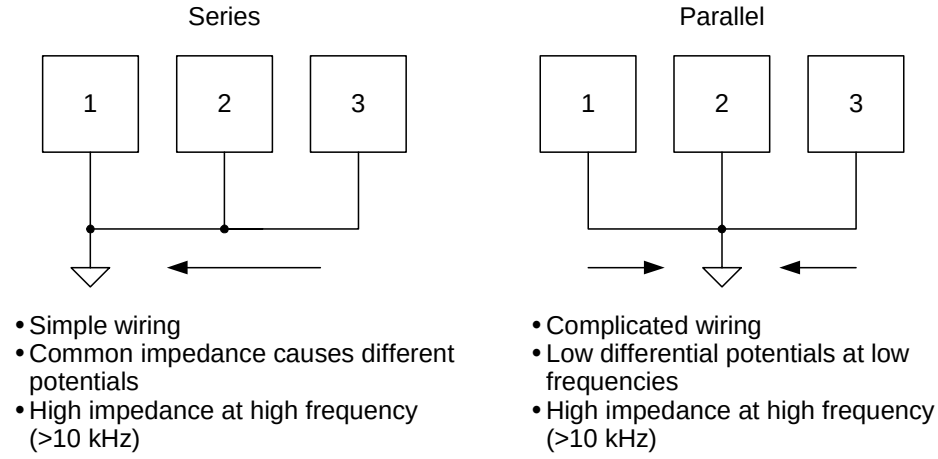


Fig. 14. Two different single point grounds.

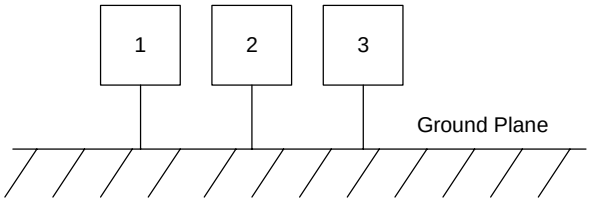


Fig. 15. Ground plane provides near ideal single point ground.

Fig. 16 shows the AC current path in a buck power stage. It is important to recognize that while the ground plane impedance is low, it is not zero so any current flowing in the ground plane generates voltages that may cause problems. In this case, it is desirable to minimize the path length between pin 2 of Q4 and the negative terminal of C3. A second high frequency current path not shown is from the control IC's gate drive terminal through Q4 gate to source and back to the control IC. Inductance in the source connection to the control IC slows switching time appreciably so that the best design would take the Q4 source connection directly to the ground plane and locate the IC as close as physically possible.

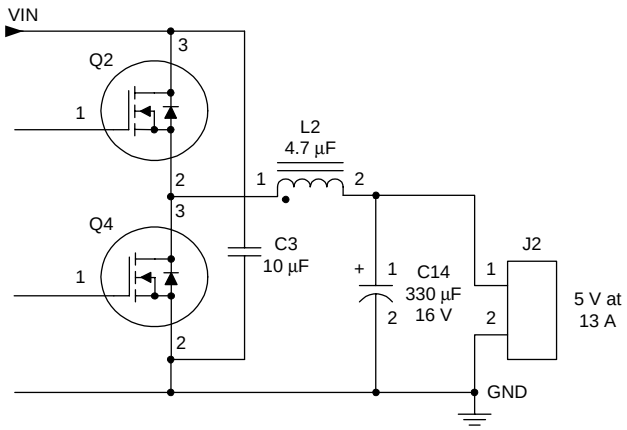


Fig. 16. Minimize high AC currents in ground plane.

An often overlooked feature of many control ICs is that pins are selected with a plan. Fig. 17 illustrates this point. All the pins on the left side of the IC are analog with a degree of noise sensitivity. If these pins are inadvertently routed near some of the more noisy pins on the right side of the control IC, sufficient noise pick-up could happen to create chaotic converter performance. So for this IC, layout all the low level passive components to the left, and place the power stage to the right of the IC. Other ICs split the analog power lengthwise, and work best with power stage and power split accordingly. A second point is that this IC has a signal ground (SGND) and power ground (PGND) to minimize interaction between the noisy power circuits and the sensitive analog circuits and best performance is found with a direct connection of both pins to the ground plane. The same thing is true for connections of bypasses and timing components, place them close together and take them directly to the ground plane.

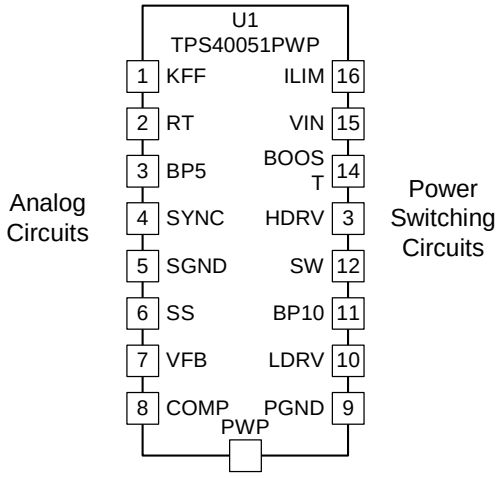


Fig. 17. Most control ICs have a planned layout.

V. THERMAL CONSIDERATIONS

One of the key layout considerations in a power supply is removing the heat from components. Historically, that meant figuring out which components generated significant heat and mounting them to a heatsink. But as the power supply becomes integrated with the system, mounting components to a heatsink is becoming less attractive and there is a move to have the PWB act as the heatsink.

There are a number of ways to move heat including conduction, convection and radiation and the power supply design uses all three. For electrical engineers, it is useful to translate the cooling process into an electrical circuit analogy. Heat can be thought of as a current source, temperature as a voltage, and conduction, convection and radiation paths can be thought of as resistances. Fig. 18 shows the electrical analog of a semiconductor dissipating heat and its cooling path. The heat, which is treated as a current source, flows from the semiconductor die through the package to an interface and then into a heatsink. Traditionally, this was a fairly easy circuit to analyze. The heat could be calculated, the semiconductor manufacturer provided the thermal resistance of the package (in ºC/W), there was characterization data on the package to heatsink interface available and the heatsink manufacturer provided its thermal resistance. So the engineer simply needs to multiply power times the sum of the thermal resistances to calculate temperature rise above ambient.

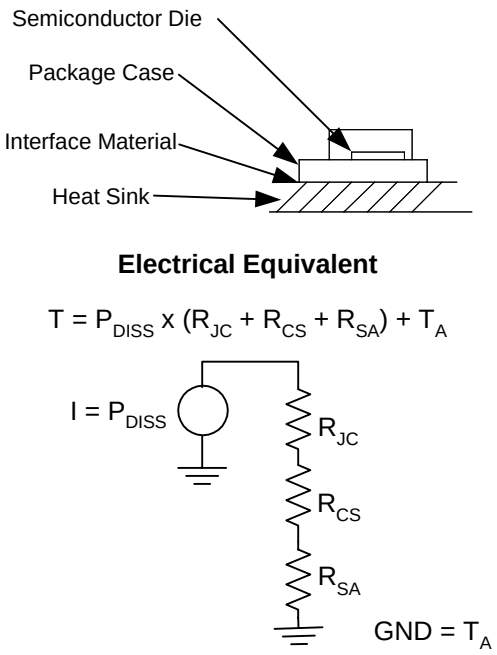


Fig. 18. Electrical equivalent circuit of heat transfer problem.

- R_{JC}: junction to case thermal resistance, usually specified
- R_{CS}: interface resistance, specified for heat sink insulators, neglectable for solder connections
- R_{SA}: sink to ambient resistance, specified for heatsinks otherwise very nebulous
- T_A = ambient

Things are changing as the power supply is tending to be integrated within a system. Fig. 19 provides a cross section of such an implementation. Rather than mounting to a heatsink, the power device is mounted to a multilayer PWB. Heat flows from the power device into the PWB where it is conducted laterally through copper conductors within the board. Cooling is provided by the surface of the PWB with both convection and radiation heat transfer. The analytical problem is greatly complicated as the only known quantities are the heat within the power device and its thermal resistance from junction to its case or to its leads. The following section provides some insight into this cooling strategy by discussing conduction heat transfer within the PWB and then convection and radiation from its surfaces.

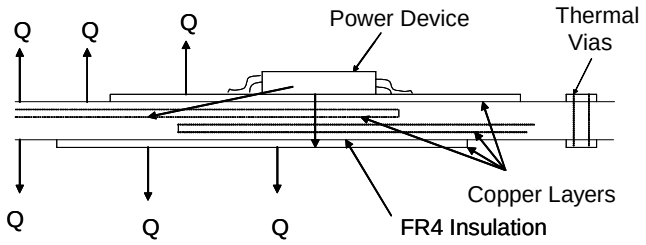


Fig. 19. Heat flow in a multilayer PWB.

To start to understand the problem, consider a typical thermal environment of an ambient temperature of 70ºC, a maximum semiconductor junction temperature of 125ºC, and a semiconductor loss of 2 W. If this semiconductor were in a power pad SO-8, its junction-to-board thermal resistance might be specified as 2.3ºC/W by the manufacturer and the calculated maximum allowable PWB temperature under the semiconductor is 5ºC – 2 W × 2.3ºC/W = 120ºC. Then consider where the heat goes from there. To a first approximation, temperature rise is proportional to power dissipation (P) and inversely proportional to surface area (Sa). The proportionality constant, h, is called the heat transfer coefficient and is about 0.001 W/cm^2/ºC (or 0.006 W/in^2/ºC) for still air. So temperature rise can be calculated using the following expression:

- Metric (cm, W, ºC)

$$\Delta T = \frac{P}{(Sa \times h)} = \frac{P}{(Sa \times 0.001)}$$

$$\Delta T = \frac{1000 \times P}{Sa}$$

$$R_{SA} = \frac{1000}{Sa}$$

- English (in, W, ºC)

$$\Delta T = \frac{P}{(Sa \times h)} = \frac{P}{(Sa \times 0.00)}$$

$$\Delta T = \frac{166 \times P}{Sa}$$

$$R_{SA} = \frac{166}{Sa}$$

We also solved for an equivalent thermal resistance (R_{SA}) as function of surface area. Note that 0.1 W of power distributed over a square centimeter, single sided surface yields about 100ºC rise (or 1 W over 1 square inch gives 166ºC rise). Applying our simple formula and solving for the area to needed to provide a 50ºC rise (120ºC – 70ºC):

- Metric (cm, W, ºC)

$$\Delta T = \frac{P}{Sa \times 1000}$$

$$Sa = \frac{P}{\Delta T \times 1000}$$

$$Sa = \frac{2}{50 \times 100}$$

$$Sa = 40$$

- English (in.,W, ºC)

$$\Delta T = \frac{P}{Sa \times 166}$$

$$Sa = \frac{P}{\Delta T \times 166}$$

$$Sa = \frac{2}{50 \times 166}$$

$$Sa = 7$$

The package is much smaller than this dimension and something must be done to provide a larger cooling surface. Either a heatsink must be used or the heat must be spread laterally in the PWB and convected through its surface.

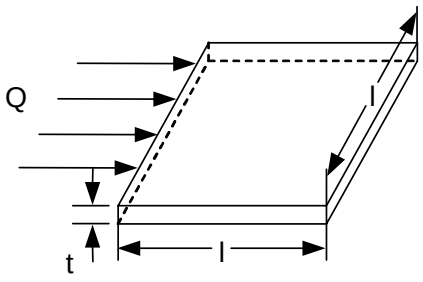


Fig. 20. Lateral heatflow is through copper conductors rather than board material.

TABLE 5. LATERAL THERMAL RESISTANCE OF A COPPER PLANE AND PWB MATERIAL

Metric	English
2-oz, 0.07-mm thick copper	**2-oz, 2.8-mils thick copper**
$R = \frac{l}{(\sigma \times l \times t)} = 1/(\sigma \times t)$ $R = \frac{1}{(0.4 \times 0.07)}$ $R = 40^{o}C/W$	$R = \frac{l}{(\sigma \times l \times t)} = \frac{1}{(\sigma \times t)}$ $R = \frac{1}{(9 \times 0.0028)}$ $R = 40^{o}C/W$
1.5-mm FR4	**0.06-inch FR4**
$R = \frac{1}{(0.00028 \times 1.5)}$ $R = 2400^{o}C/W$	$R = \frac{1}{(0.007 \times 0.06)}$ $R = 2400^{o}C/W$

Lateral thermal resistance is much like electrical resistance and can be calculated as shown in Fig. 20. (For reference other thermal conductivities can be found in the appendices). The resistance is increased by length and reduced by cross sectional area and thermal conductivity. Two possible paths are presented in the figure, through the PWB material and through a copper layer in the PWB. A 1.5-mm (0.06-in) PWB is compared to a 0.07-mm (0.0028-in) thick copper plane. Even though the PWB material is much thicker then the copper, the high copper thermal conductivity makes it a much lower resistance path for heat flow. The strategy to use the PWB surface as the cooling surface must include making use of the copper within the board to spread the heat. Also, note that just as with the electrical resistance of conductors, you can count squares of thermal conductors to estimate the thermal resistance from point to point.

The next possible path to consider is through the PWB to the other surface. Fig. 21 shows the calculation for two 2.54-cm (1-in) square planes separated by 1.5-mm (60-mil) PWB thickness, (board front to back). The low thermal conductivity of the board is offset by the large area and short path length and thermal resistance of 8ºC/W is calculated. This number is small compared to the 166ºC/W board to air resistance so heat is dissipated from both sides of board.

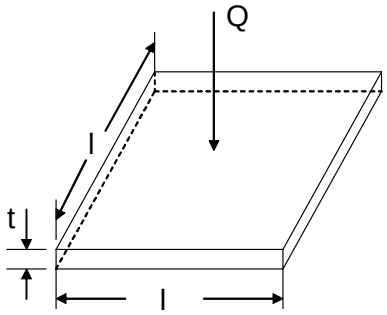


Fig. 21. Specific thermal resistance through board is much less than board-ambient.

$$R = \frac{t}{(\sigma \times A)}$$

$$R = \frac{1.5}{(0.00018 \times 2.54 \times 2.54)} \quad \text{Metric}$$

$$R = \frac{0.06}{(0.007 \times 1)} \quad \text{English}$$

In some cases, a heatsink is affixed to the backside of the PWB and heat is transferred through the board into the heatsink. Sometimes this thermal resistance may be too high. Vias offer a method to further reduce the side-to-side thermal resistance. A few vias can halve the thermal resistance from board front to back, and a large number can reduce the thermal resistance down to the 1ºC/W range. Fig. 22 shows a typical via and provides the calculation of its thermal resistance. For this sample via, thermal resistance is about 100ºC/W and it only takes 12 of these in parallel to halve the thermal resistance through the PWB board material. Solder filling or further plating can yield significant improvement over this number.

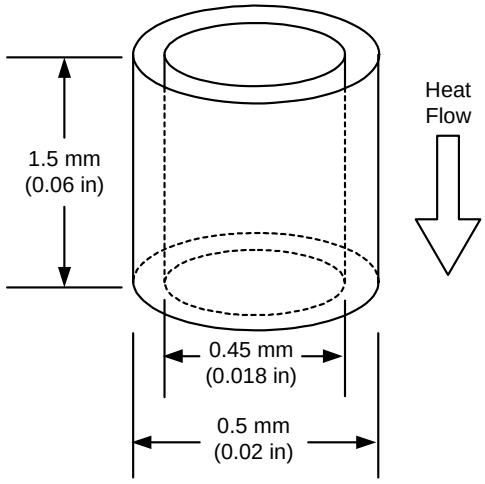


Fig. 22. A single via has about 100ºC/W thermal resistance and they can be paralleled.

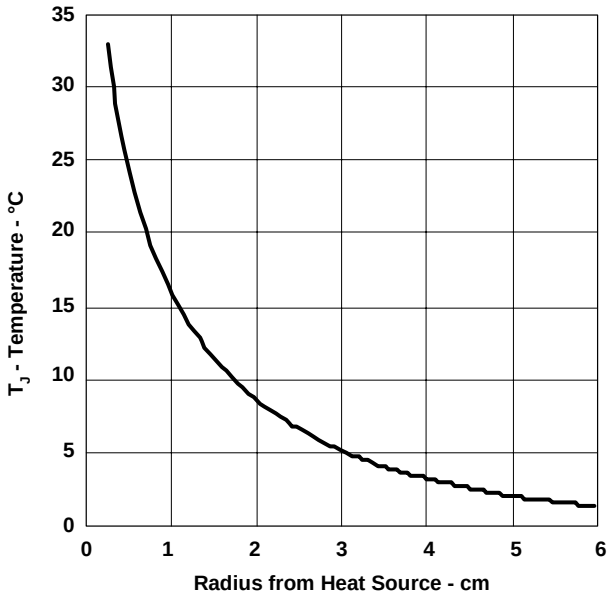
$$R = \frac{l}{(\sigma \times A)}$$

$$R = \frac{l}{(\sigma \times \pi \times (r_o^{\,2} - r_i^{\,2}))}$$

$$R = \frac{1.5}{(0.4 \times \pi \times (0.25^2 - 0.225^2))}$$

$$R = 100^o C/W$$

The general formula for conduction and convection heat transfer can be combined to solve for the temperature rise. The following calculations were based on a 2-W heat source with 5 mm (0.2 in) diameter which mimics a power pad S0-8 device. To solve for the heat rise, the use the axial symmetry of the situation and construct a ladder network of resistors driven by a current source of 2 W. The current source drives a series resistance determined by the lateral thermal resistance of the board which can be calculated as $R_{CON} = \ln(Ro/Ri)/(2 \times \pi \times 0.4 \times 0.07)$ Metric or $R_{CON} = \ln(Ro/Ri)/(2 \times \pi \times 9 \times 0.0028)$ English. The 2 in the equation assumes that there is a copper plane on top and bottom of the board, the expression neglects front-to-back thermal resistance. At the output of the resistor are two more resistors, one connected to ground (or really ambient temperature) and the second representing the thermal resistance of the next annulus. The resistance to ground is calculated from the heat transfer expression as $Rconv = 1000/(Ro^2 - Ri^2) \times \pi/2$ Metric or $Rconv = 166/(Ro^2 - Ri^2) \times \pi/2$ English. The circuit was then put in Excel and the temperature rise was calculated as shown in Fig. 23. A calculated temperature rise about 35ºC is shown and even on infinite board most of the heat is dissipated in the first inch from heat source. This is consistent with our calculated needs of seven square inches of dissipating area to control temperatures. This is also about the best one can do with PWB surface cooling with no air flow. The calculated thermal resistance is about 15ºC/W in this case. Practical experience tends toward a more conservative 20ºC/W to 30ºC/W.



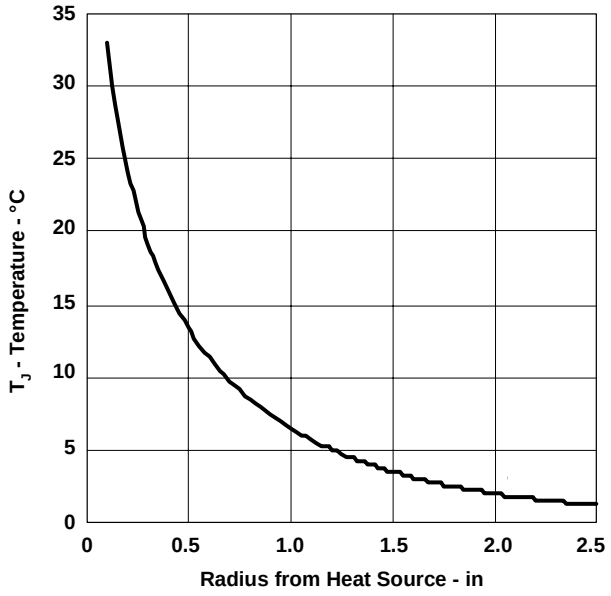


Fig. 23. 2 W of dissipation on double sided board calculates 30ºC rise.

One more thermal path that needs to be considered is across a break in a plane. Fig. 24 presents an approximation. It provides the thermal resistance of a 0.25-mm (0.01-in) break that is 2.54 cm (1 in) wide and the conclusion is that very little heat takes this path. One way around this issue is to use buried planes or a plane on the other side of the board to bridge this gap. The vertical heat flow can be good if there are large areas involved on both sides of the board.

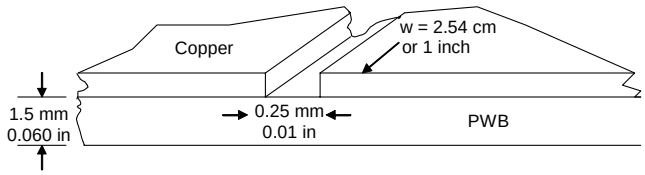


Fig. 24. Thermal resistance gap significantly adds to temperature rise.

$$R = \frac{l}{(\sigma wt)}$$

$$R = \frac{0.25}{(0.00018 \times 25.4 \times 1.5)} \text{ Metric}$$

$$R = \frac{0.01}{(0.007 \times 1 \times 0.06)} / \text{English}$$

$$R = 36^{o}C/W$$

There are more precise expressions for convection heat transfer. One of the more popular one recognizes that h is not constant but is a function of size and temperature rise as shown in the following. With a little manipulation, the equation can be resolved for temperature rise.

$$\Delta T = \frac{Pd}{(h \times A)}$$

$$h = K\left(\frac{\Delta T}{\sqrt{A}}\right)^{1/4}$$

$$\Delta T = \frac{Pd}{\left(K\left(\frac{\Delta T}{\sqrt{A}}\right)^{1/4} \times A\right)}$$

$$\Delta T^{1.25} = \frac{Pd}{(KA^{7/8})}$$

$$\Delta T = Pd^{0.8} \times \frac{K'}{A^{0.7}}$$

$$\Delta T = P^{0.8} Sa^{-0.7} \times 650^{o}C \ cm,W$$

$$\Delta T = P^{0.8} Sa^{-0.7} \times 100^{o}C \ in,W$$

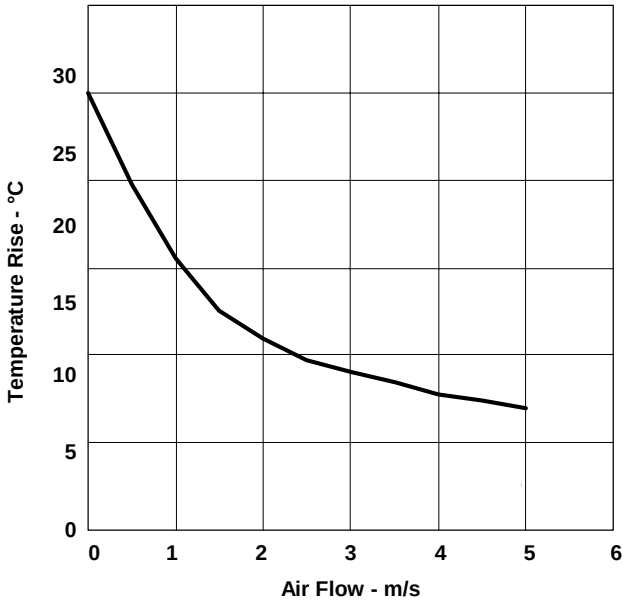
Finally, *h* is not constant with orientation. A vertical surface cools better than a horizontal surface, as shown in Table 6.

TABLE 6. VALUES OF K′ FOR VARIOUS ORIENTATION

Surface Orientation	K′ (In cm. ºC, and W)	K′ (In in. ºC, and W)
Vertical	650	100
Horizontal plane, top surface	675	104
Horizontal, bottom surface	1375	204

To summarize, to make use of the PWB as a cooling surface, a low-lateral thermal resistance is needed. It can be obtained with large, thick copper planes to distribute heat across PWB surface. It is best to minimize the thermal resistance with as much copper on each layer as practical. The thermal resistance from side to side of the PWB is low enough that it is practical to count on both sides of the board to cool. If further reduction of thermal resistance through the board is needed, substantial improvements can be made with thermal vias. Also, minimize breaks in planes as they substantially degrade lateral heat flow. Adjacent planes bridging the necessary breaks can also improve the lateral heat flow.

So far only natural convection has been discussed, but many systems incorporate fans to provide improved heat transfer. And the impact can be dramatic as shown in Fig. 25. Even a whisper of air can reduce temperatures. This curve was generated from heat sink data and shows that a 25ºC rise can be diminished to 5ºC with airflow. Airflow is measured in meters/second (or linear feet per minute) over the surface. For reference for those using our confusing English dimensions, 1 mile per hour is 88 feet per minute. Typical system airflows in the 0.5 ms to 2 ms (100 to 400 feet per minute) can provide a 2-to-1 temperature reduction at the pace of a leisurely walk!



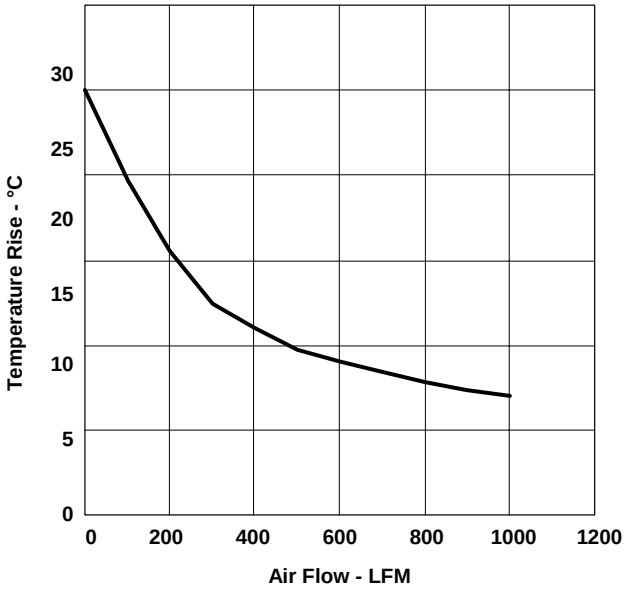


Fig. 25. Even a whisper of airflow can dramatically lower temperature rise.

Radiation may also take some heat out the board, but for this to occur, the board must "see" a lower ambient temperature. An interior PWB with adjacent boards of similar temperatures is unable to dissipate heat by radiation. The heat radiated can be calculated with the following general formula. This calculates the radiation heat transfer between two surfaces of temperature T1 and T2. Note that these are absolute temperatures so that room temperature is 273 + 25 = 298ºK. The first constant contains emissivity and a unit's correction factor. "*A*" represents the surface from which the heat is transferred; *Fz* is an emissivity factor which is the ratio of the materials ability to radiate heat compared to a black body. (Note that one can not visually inspect a surface to determine if it is a black body as most of the heat will be radiated at infrared frequencies). And *Fa* is a configuration factor, or form factor, that relates to how the two surfaces see each other.

$$q = \sigma \times A \times F_{\varepsilon} \times F_{a} \times (T_1^4 - T_2^4)$$

- σ = constant
- A = area
- F_Z = emissivity factor
- F_A = configuration factor
- T = temperature degress kelvin

This equation was then set up for a unit area, 0.6 emissivity radiator in a very large room at 70ºC. The temperature of the radiator was varied and the heat transfer was calculated as shown in Fig. 26. The heat transfer is almost linear with temperature. This can be explained by expanding the expression $(1+x)^4$ and making the assumption that x is small compared to 1. All the higher order terms drop out and the expression is linear in x or temperature rise or:

$$(1+x)^4 = 1 + 4x + 6x^2 + 4x^3 + x^4$$

$$x << 1$$

$$(1+x)^4 \approx 1 + 4x$$

This allows the calculation of an equivalent thermal resistance per unit area of 55ºC/0.04 = 1400ºC/W/cm^2 (or 55ºC/0.25 W = 220ºC/W/in^2) which is approximately twice natural convection cooling or simply put, radiation cooling at typical board temperatures is about ½ as effective as natural convection. Rather than complicating the convection calculations by adding this in, most designers choose to use this as a safety factor.

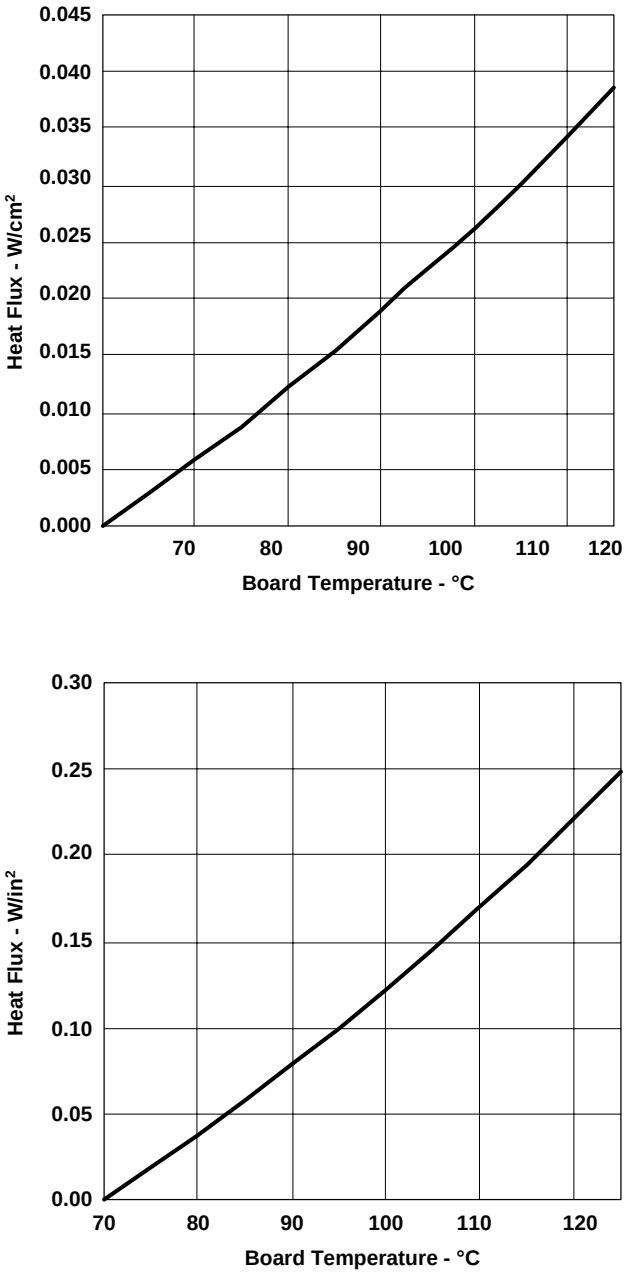


Fig. 26. Radiation heat transfer provides safety factor over convection calculations.

VI. Design Examples

The following figures provide some real world examples of what to do and not to do when laying out your power supply. Fig. 27 presents a good EMI filter layout. The points to be noted are; the integrity of the common inductor is maintained by not having board capacitance short it out, in other words, T2 inputs pins do not cross outputs pins. Also there is no ground plane under EMI filter to short across the common mode inductor. Also, wide, short trace are used to minimize losses and wide spacing between traceses meets high voltage requirements and minimize coupling capacitance.

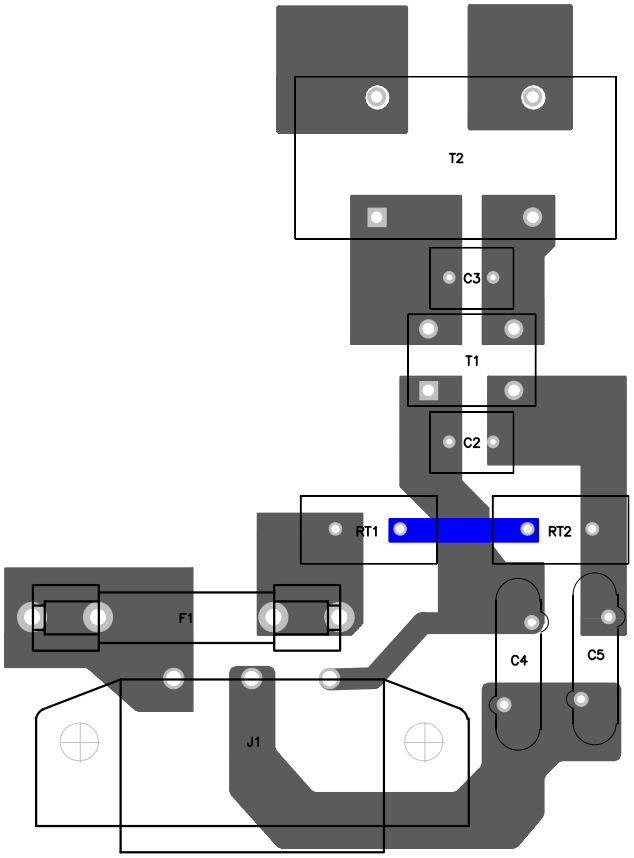


Fig. 27. Example EMI filter layout.

Fig. 28 and Fig.29 shows both a right way and a wrong way to connect output capacitors. The right way minimizes the series inductance of the output filter capacitors. Current is routed directly under the high frequency capacitor, C39. Lead lengths connecting the capacitors are minimized to reduce series inductance. Although not apparent on these pictures, numerous vias were dropped into the ground plane on the bottom of the board.

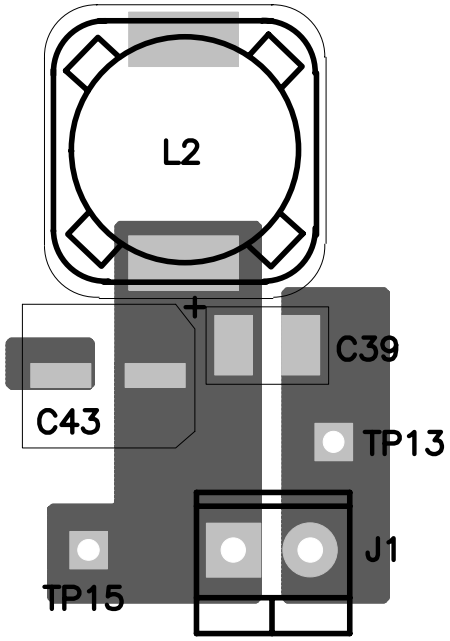


Fig. 28. Proper output filter routing reduces high frequency ripple (low series inductance).

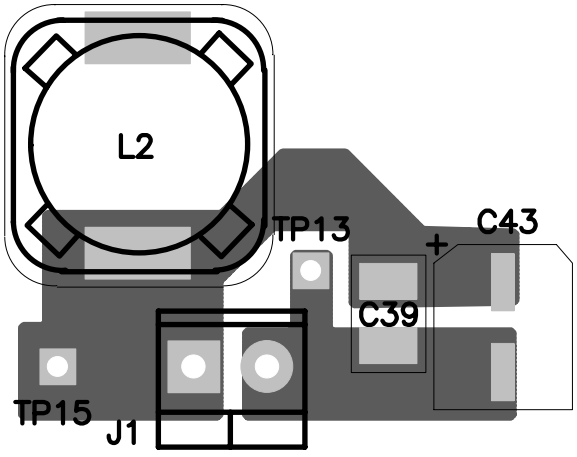


Fig. 29. Proper output filter routing reduces high frequency ripple (low series inductance).

Fig. 30 and Fig. 31 shows the right and wrong way to connect the output voltage sense point. In the right way, shown on the left, the sense point is connected as close to the load as possible. The wrong way just connects to the most convenient point. With current flow between this connection and the load, there is voltage drop in the PWB which degrades regulation. A careful designer will review this connection closely as most layout people go for convenience every time.

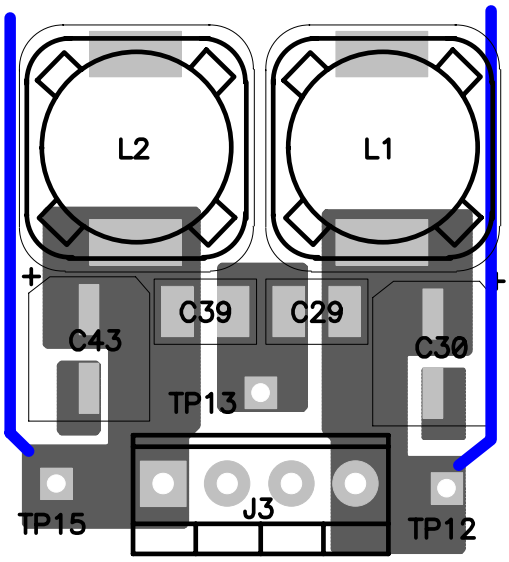


Fig. 30. Proper sensing improves load regulation.

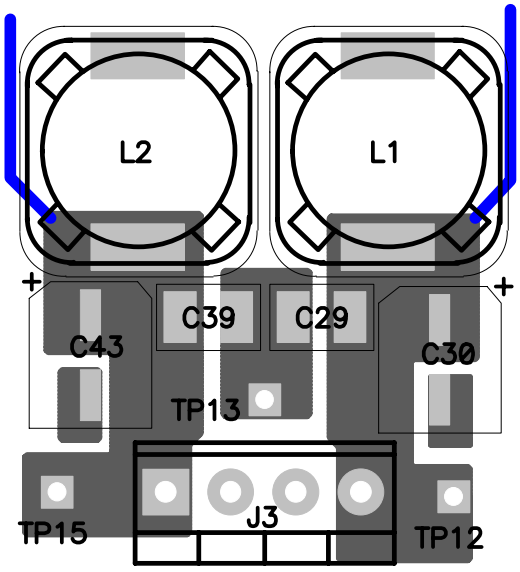


Fig. 31. Proper sensing improves load regulation.

Fig. 32 shows a good layout for the error amplifier and low level components on the left side of the controller. It has very short trace runs to minimize parasitic capacitance and switching noise pick-up. Very close attention is paid to the error amplifier connections (pins 7, and 8) which are extremely noise sensitive and were routed carefully. This is a multilayer board and the second layer is ground plane to minimize pick-up and inductance. The design drops returns into the ground plane without long traces. Feedback from the output voltage is routed well away from switching power signals.

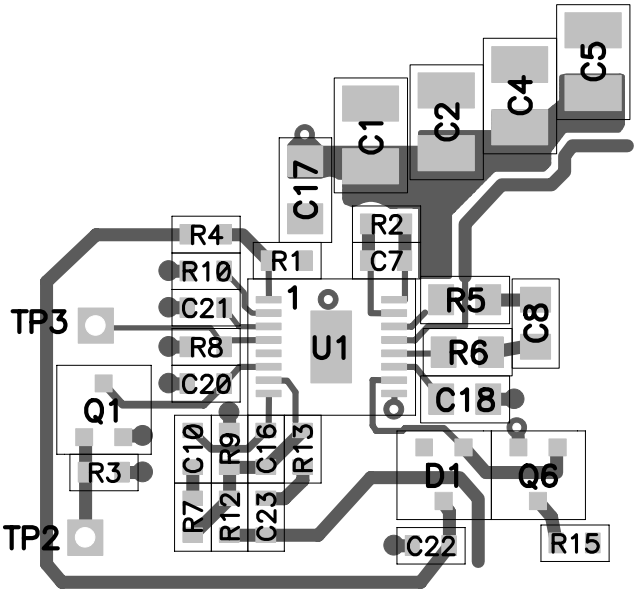


Fig. 32. Proper layout control minimizes checkout issues.

Fig. 33 is an example of good input bypass capacitor layout. C2 and C100 input caps, ground side drops into the ground plane through multiple vias. Also, the bottom FET (Q6) ground drops into the ground plane through multiple vias. And on the bottom layer, there is a solid uninterrupted ground plane. Also, note that the ground connections for these two power parts are made in close proximity to minimize high AC current in the ground plane.

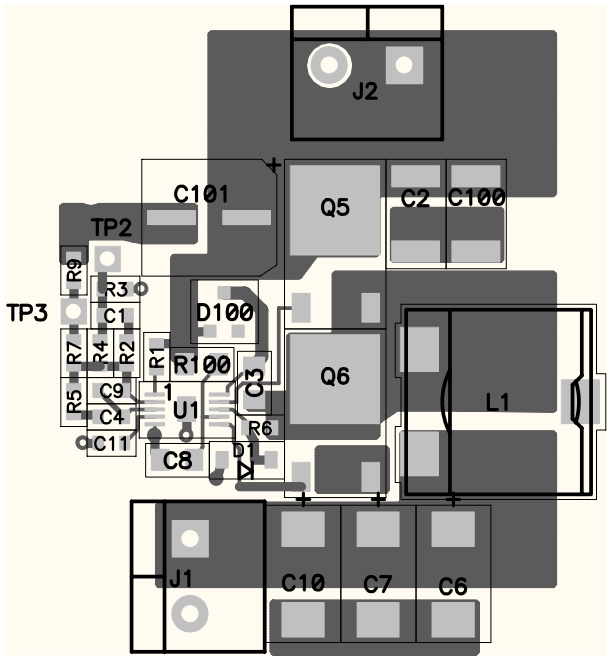


Fig. 33. Proper input capacitor placement provides short path for AC current.

Fig. 34 presents a high dissipation example. Here, a large surface was used to dissipate the heat from the power components. Spreading the heat required the designer to maximize copper in the available space. This was a multilayer board and this copper pattern was duplicated on several layers. There were very few breaks in the copper leading to good lateral spreading. Thermal vias were located near and under heat sources to help spread the heat to the back of the board and internal layers.

Fig. 34. Massive copper pours help spread heat.

Fig. 35 presents a successful job of cooling a power supply through the PWB surface. FETs with about 1 W of dissipation were cooled to a 50 degree rise by using the methods presented in this article. Copper planes helped to stabilize temperatures across the board surface and a large number of vias provided a good front to back thermal path. Power components and their dissipations were spread out over the board surface to help equalize the heat flow from the board surface to the ambient FETs closest to the edge of the board were the hottest as they had the least available board area for cooling.

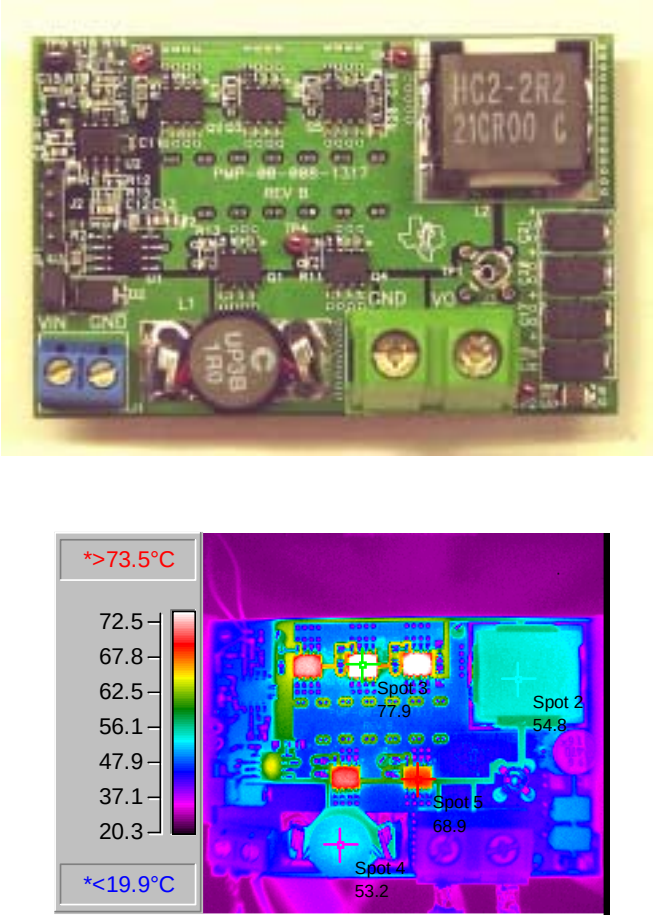


Fig. 35. Attention to details yields a well cooled design.

VII. Summary

Power supply layout is as important as any other design consideration. The power supply engineer must be involved in the parts placement and routing. An understanding of AC and DC parasitics, grounding, and cooling makes a successful design.

References

[1] Henry Ott, *Noise Reduction Techniques in Electronic Systems*, John Wiley and Sons, 1988

[2] John Holman, *Heat Transfer*, McGraw-Hill, 1968

[3] Paul Davies, *Thermal Management in Power Supply Design*, Powercon 10, 1983

[4] IPC-2221A, *Generic Standard on Printed Board Design,* IPC, 2003

[5] Abe Pressman, *Switching Power Supply Design*

[6] Fredrick Grover, *Inductance Calculations, Working Formulas, and Tables*, Dover, 1962

[7] John Kraus and Keith Carver, *Electromagnetics*, McGraw-Hill, 1973

APPENDIX A.
THERMAL CONDUCTIVITY OF OTHER MATERIALS

Material	W/(cm ºC)	W/(in ºC)
Air	0.0002	0.0007
Alumina	0.2	0.9
Aluminum	1.8	4.4
Beryllia	1.6	4
Copper (OFC)	3.6	9
Epoxy (PC board)	0.003	0.007
Ferrite	0.04	0.10
Steel	0.15	0.60
Tin-lead	0.4	1.00

APPENDIX B.
SAMPLE EMISSITIVITIES

Material	Emissitivity (e)
Bare aluminum	0.08
Polished copper/tin	0.04
Glass	0.9
Anodized aluminum	0.8
Lacquer	0.8
Water	0.95
White alumina	0.88
Machined copper	0.7
Dull nichel plate	0.11

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265