Ultra-Thin Silicon Beam Lead Chips for Superconducting Terahertz Circuits

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Abstract. We present a process for fabricating THz superconducting circuits on ultra-thin (4um and less) silicon chips. The chips feature gold beam-leads, and are designed to accommodate RF filter structures, and either SIS junctions or hot-electron bolometers as the non-linear circuit element. The beam leads provide electrical connections, thermal contact, and physical support for the chip within a waveguide. Our approach begins by fabricating the superconducting circuit and beam leads atop the device layer of a silicon-on-insulator (SOI) substrate. The chip is then mounted, device side down, atop a quartz carrier wafer. A combination of mechanical lapping and chemical etching removes the handle silicon. Using backside photolithographic alignment through the quartz carrier, a thick photoresist is patterned on the exposed device silicon. The individual chips are then defined in a reactive ion etch of the device silicon, which is terminated after the quartz carrier and gold beam leads are exposed. The combination of superconducting mixers technology and silicon-micromachining techniques promises to open up the THz regime to large format spectroscopic imaging arrays. The potential for such systems are multiple; examples include atmospheric research, astrophysics, and security systems.

1. Introduction

Superconducting devices for THz applications are often fabricated on thin quartz chips, which are then fitted into metal waveguide structures. Early designs had the chips resting on the bottom of the waveguide. As a result, around half of the waveguide is occupied by quartz while the upper volume is air. Ideally, the presence of the dielectric

is minimized and the entire waveguide volume is of a uniform, and minimized, dielectric constant. To achieve this, designers rest very thin chips (less than 50nm) along shoulders milled into the waveguide, thereby minimizing the volume of chip within the waveguide while still situating the metalized circuitry in the waveguide center [1]. However, quartz chips may only be thinned to around 25um before becoming too brittle. Our work aims to overcome this limitation by substituting ultra-thin silicon for the quartz.

The electrical contact between the superconducting circuitry and external RF and IF connections are typically made via wire bonds, solder bumps, conductive gaskets or micro-springs [2,3]. Such techniques are not possible when using silicon that is only a few microns thick as the chip would rupture when making such connections. To overcome this, we have devised a scheme for maintaining electrical and thermal contact from the chip to the waveguide block via beam leads, which extend from the perimeter of the chip. The mechanical rigidity of the beam leads is designed to support the chip between two halves of a waveguide block such that the chip is suspended within the middle of the waveguide channel. Beam leads have been employed in RF applications, most notably in GaAs-based mixers and multipliers [4-5]. They have also been demonstrated on quartz substrates designed for superconducting SIS-based mixer applications [6,7]. Beam leads are robust enough to handle the rigors associated with mixer assembly, even when extended several hundred microns beyond the perimeter of the chip.

Silicon offers several advantages over quartz for THz applications. The thermal conductivity of silicon is much higher; 150W/mK versus 2W/mK. The rupture modulus of silicon is also greater than that of quartz; 135MPa versus 50MPa. As a result, silicon may be thinned much more so than quartz before it becomes too brittle to handle. On the other hand, silicon has a larger dielectric constant than quartz, 11.9 versus 3.8 at 10GHz, and a dielectric loss tangent that is nearly 40 times larger.

We have conducted numerous analytical studies on the feasibility of using ultra-thin chips in THz receiver applications in both single-chip receivers and array antenna structures [8]. The use of a silicon chip as the substrate for THz circuitry greatly simplifies the RF design process. In addition, since shoulders do not need to be milled within the waveguide channel to accommodate a chip with 1um thick beam leads, machining of the receiver block becomes much more straightforward.

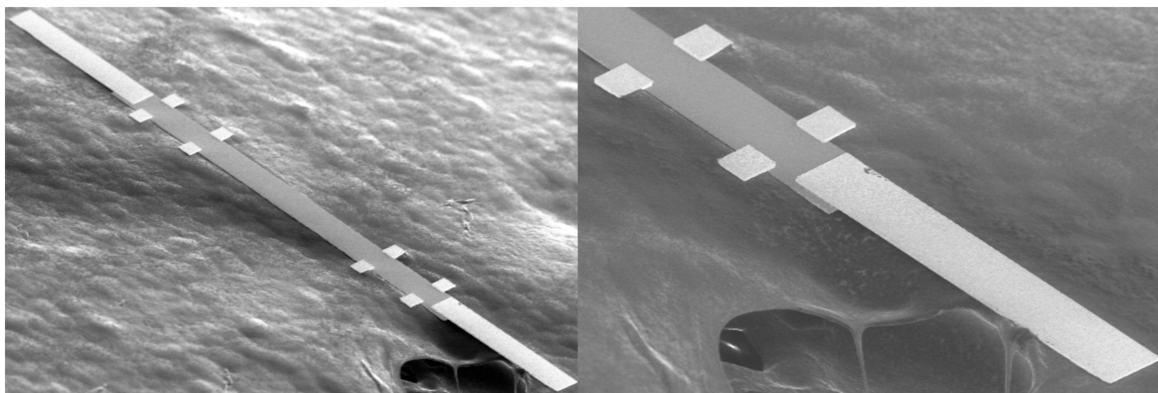

Figure 1. Shown are two SEM micrographs of an ultra-thin silicon chip with gold beam leads fabricated at UVa. Ultra-thin silicon chips allow for a low dielectric profile within a receiver waveguide. The beam leads provide electrical, thermal and mechanical contact from the superconducting circuitry on the chip to the receiver block. The entire chip length is less than 1.2mm.

2. Fabrication

The process for fabricating ultra-thin silicon chips with beam leads is broken down into three subsection: beam lead fabrication, silicon thinning, and chip definition. For this work, seven sets of silicon chips were fabricated in order to investigate variations in silicon and beam lead thickness. To simplify sample preparation, none of these chips feature submillimeter-wave circuitry such as RF filters, antennas, or active superconducting elements. We have, however, separately fabricated working Nb based HEB bolometers on SOI wafers. When fabricating chips with such circuitry, the fabrication steps for these elements are performed between the beam lead fabrication and silicon thinning subsections [9].

Each set of silicon chips is defined from a square SOI wafer measuring 1.9cm on a side. An SOI wafer consists of three layers; a thick handle silicon on the bottom, followed by a buried oxide layer (BOX), and then a thin device silicon layer on top. It is from the device silicon from which the ultra-thin chips are defined. For this work, three different device layer thicknesses are investigated; 1.6um, 3.0um and 4.0um (Virginia Semiconductor Inc., Ultrasil Co). The BOX layer for the first two is 1.0um thick, +/- 5% and that of the third is 1.5um thick, +/- 5%. Handle thickness varies from 350um to 500um, +/- 50um.

2.1 Beam lead fabrication

Electroplating is used to fabricate gold beam leads atop the device silicon. The beam leads vary in thickness from wafer to wafer, and range in thickness from 0.2um to 4.5um. Prior to plating, a seed layer is deposited atop the device silicon using DC magnetron sputtering in a multitarget deposition system with a base pressure of 10^{-8} Torr. The seed layer ensures electrical continuity across the wafer, and consists of 10nm of titanium below 50nm of gold. The titanium serves as an adhesion layer between the device silicon and the gold. An ion mill is performed for two minutes prior to titanium deposition in order to promote adhesion between the titanium and the device silicon.

The beam lead structures are defined using AZ4330 positive photoresist and an i-line contact mask aligner. Spun at 3krpm, the resist is 4um thick, allowing for several microns of spacing between the top of the thickest beam leads and the top of the resist. After developing, a three minute exposure to an oxygen plasma (100W, 1Torr) cleans the gold surface of any remaining organics prior to the plating process. Following resist patterning, the beam leads are plated atop the gold seed layer using Techniq 25E plating solution. Afterwards, the resist is removed with acetone. The gold seed layer is removed using an iodine-based wet etchant and the titanium adhesion layer is etched away in a dilute HF-based wet etchant.

2.2 Silicon thinning

After the beam leads are fabricated, the handle silicon is removed from the backside of the wafer. This is done in a two step process. The handle is thinned to 30um microns in the first step by mechanical lapping. The remaining 30um of handle silicon is removed with a silicon wet etch process.

Prior to thinning, the silicon wafer is mounted beam lead side down atop a 250um thick quartz carrier. The quartz carrier serves as a rigid support for the wafer, which losses most all of its mechanical rigidity after the handle silicon is removed. A thin layer of clear mounting wax adheres the wafer to the carrier. The quartz carrier and clear mounting wax allow for a subsequent backside alignment process, which is necessary for aligning the chip extents with respect to the beam leads.

Next the wafer/carrier pair is mounted atop a thick metal lapping block using the same wax. The wafer and carrier are then planarized with respect to the lapping block by placing all three into a mechanical pressure jig [10]. With the wafer, carrier and lapping block inside, the jig is heated to an internal temperature of 120C, allowing the wax to melt. Pressure is then applied to the jig, which is then cool to solidify the planarized wafer and carrier atop the lapping block. After cooling, the pressure is released and the wafer is ready for the first step of the thinning process.

The majority of the handle silicon is removed by mechanical lapping. Our lapping system consists of a Techprep Polishing Machine and a Multriprep Positioning Device, both of which are made by Allied High Tech Products, Inc. A 30um grit diamond lapping film is used to reduce the handle silicon to 30um +/- 10um above the BOX layer in approximately one hour. Afterwards, the carrier and wafer are removed from the lapping block.

The remaining handle silicon is removed by a silicon wet etch solution. TMAH (tetramethyl ammonium hydroxide, $(CH_3)_4NOH$), diluted to 8% by weight in de-ionized water and heated to 60C +/- 3C [11]. The BOX layer serves as an etch stop; the high selectivity of the TMAH etchant between silicon and silicon dioxide ensures that the underlying device silicon is protected from the etch solution by the BOX layer.

In order to prevent the etchant from seeping under the wafer and attacking the device silicon, the wafer and carrier are placed in a jig that prevents the etchant from contacting the wafer sides. The mounting wax is highly susceptible to the TMAH etchant, especially at elevated temperatures. If the wax is exposed to the etchant, etchant will seep under the wafer and damage the device silicon. The jig prevents contact between the etchant and the device silicon by sealing the wafer along its perimeter with a silicone rubber seal.

Due to the uncertainty in the handle thickness after mechanical lapping, etch times range from 3 to 4.5 hours. A peristaltic pump re-circulates fresh etchant to the etch surface. The etch rate is highly dependant upon temperature, and increases considerably with higher etchant temperature [12,13]. However, the etchant must be maintained at a temperature no higher than 60C because the clear mounting wax will soften and re-flow at temperatures beyond 70C. When the wafer is thinned to within a few microns of the combined BOX and device silicon thickness, the membrane becomes extremely delicate, and is likely to crack and peel if perturbed by flowing wax.

2.3 Chip definition

After the handle silicon is removed, an etch mask is patterned on the backside of the wafer in preparation for etching of the device silicon. The etch mask defines the individual chip extents, and so must withstand the high energy ion bombardment and chemical attack associated with the reactive ion etch of the device silicon.

The reactive ion etch conditions are 11.7sccm of CCl_2F_2, 13.5sccm of SF_6, 7sccm of Ar, 30mT pressure and 0.3W/cm^2 RF power. Etching of silicon with this chemistry is discussed in detail by Rangelow, et al [14]. For the same reasons discussed in association with the TMAH etch of the handle silicon, the etch conditions in the RIE chamber are controlled to prevent the wafer from heating beyond the melting point of the mounting wax. To prevent excess heating, the platter of the RIE is cooled to 8C. In addition, the RF power is cycled such that it is on for one minute and then off for two minutes, allowing the sample to cool after the brief etching time. As a side effect of cooling however, the etch rate of the device silicon is reduce considerably compared to results presented in Rangelow; we find an etch rate of the device silicon of 126nm/min with a standard deviation of 3nm/min when using a photoresist mask.

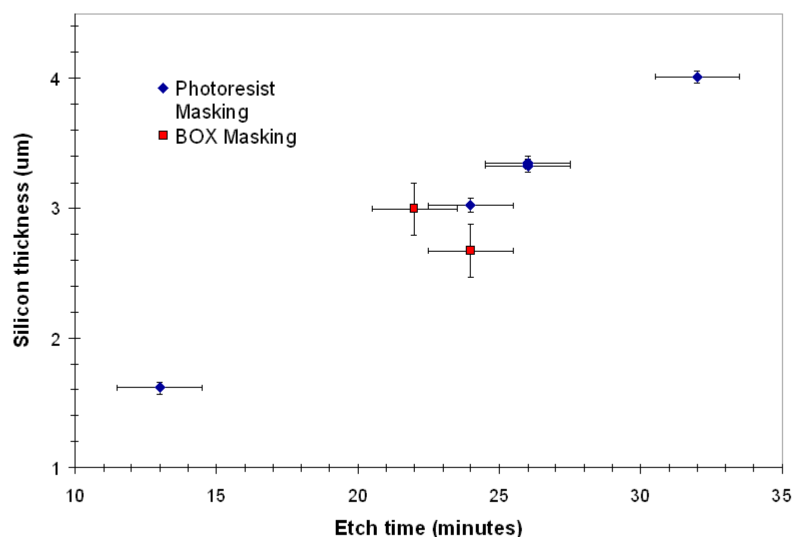

Figure 2. Etch time versus silicon thickness is dependant upon the type of mask used during reactive ion etching. Photoresist masks are more durable, and do not degrade during the etch process. As a result, the distribution of chip thickness is small, around 50nm. Etching with a BOX mask leads to greater distribution in the final chip thickness due to rapid depletion of the BOX layer; standard deviation is around 200nm.

Two masking methods were developed for the reactive ion etch of the device silicon. Both of these are designed to withstand the conditions associated with removing several microns of silicon in the Rangelow etch. The first masking method takes advantage of the BOX layer present atop the device silicon. In the Rangelow chemistry, silicon dioxide etches at a rate of approximately one third that of silicon. Therefore, using a 1um BOX layer mask will result in a chip thickness of 3um, so long as the original device silicon thickness is greater than or equal to 3um and the RIE process is uniform enough to minimize over-etching. Backside photolithography is used to define AZ5214 photoresist atop the BOX layer. Exposure to an HF-based wet etchant removes the exposed BOX layer. Next, the resist is dissolved in AZ400k developer (undiluted), leaving behind the patterned BOX layer. The BOX layer is then completely removed during the subsequent RIE process.

The second masking method does not rely on the BOX layer, which instead is removed completely by an HF-based wet etchant prior to photoresist patterning. In order to withstand the RIE conditions, a photoresist mask several microns thick is patterned on the exposed device silicon. For this work, we used both AZ4330 and AZ4620 photoresists. Both are able to withstand the extended etch periods and energetic etch conditions associated with the Rangelow etch. The AZ4330 is spun on to a thickness of 4um, which is sufficient for masking device silicon that is 3um thick or less. For thicker device silicon, the AZ4620 is used, which is spun on to a thickness of 7um. The etch rates of each of these resists is around 80nm/min. After the etch, the remaining resist is removed using a combination of O_2 plasma etching and exposure to undiluted AZ400k.

Etching results using these two masking processes are different in a number of notable ways. First, the wet etch process used to define the BOX masking pattern results in a tattered etch mask perimeter. These errors are transferred to the device silicon during the RIE, resulting in ill-patterned chips. Another problem associated with the

BOX method is lateral under-etching of the device silicon during the RIE process. Lateral under-etching is prevented in the photoresist process by sidewall deposition of fluorinated polymers. It is believed that the polymeric photoresist is disassociated during the RIE process, allowing for polymerisation of hydrogen, carbon and ionized fluorine along the sidewalls of the etched silicon [15]. The sidewall polymerizations prevents chemical attach of the silicon, thereby preventing the etching of silicon below the photoresist mask. A third difference between the two masking processes is shown graphically in Figure 2. A 200nm standard deviation in final chip thickness is associated with the BOX-based etching. Contrasting, the photoresist masks produce a standard deviation of no more than 50nm for a given wafer. The difference is associated with the rapid etching of the BOX mask and the variations in etch rate across a wafer. It takes on average three minutes for an entire chip to be etched through to the carrier wafer after the first part of the wafer shows evidence of being complete. This variation in etch rate results in variations in final chip thickness since the BOX masking patterns are removed prior to completion of the etch. The chips masked with photoresist do not demonstrate such large variation in thickness since several microns of photoresist are designed to remain atop the device silicon after the etching is complete.

After etching, the individual chips are removed from the quartz carrier by rinsing in acetone, which dissolves the mounting wax. The chips are separated from the carrier and float free within the acetone-filled beaker. The chips are then collected by flowing the acetone through filter paper. A light rinse with methanol removes any remaining organic debris atop the chips.

3. Discussion

Seven batches of silicon chips, with thickness ranging from 1.6um to 4um, were fabricated for this work. A summary of specifications for these batches is listed in Table 1. Chip yields are greater than 90%. With the exception of one batch, the silicon chips from each batch measure 76um by 800um. The chips from batch 30508S, which are of a different design, are 500nm by 2mm. In all cases, the chips are durable and withstand the rigors of receiver block assembly. None of the samples are too brittle to handle; the large chips from batch 30508S were also the thinnest, measuring just 1.6um thick.

All of the samples presented in this work were fabricated with thick gold beam leads extending from the perimeter of the silicon chips. Functional beam lead thickness ranges from 1um to 5um thick and extend up to 260um beyond the perimeter of the chip. Batch 30702SD was fabricated with 200nm thick beam leads, which were found to be to thin to maintain shape. The 200nm beam leads are foil-like, lacking the springiness associated with the thicker beam leads. It may, however, be possible to fabricate beam leads as thin as 200nm by substituting sputtered or evaporated gold for the plated gold.

Table 1.

Sample	Beam Lead Thickness	Silicon Thickness	RIE Mask Type	Comments
30508S	4.5um	1.6um +/- 30nm	Photoresist	
30625SB	1.5um	3.0um +/- 203nm	BOX	Large variation Si thickness
30625SD	2.7um	2.7um +/- 32nm	BOX	10% over-etch of Si
30702SA	1.9um	3.0um +/- 34nm	Photoresist	
30702SB	1.1um	3.3um +/- 54nm	Photoresist	
30702SD	0.2um	3.3um +/- 13nm	Photoresist	Beam leads too thin
30714SB	1.5um	4.0um +/- 16nm	Photoresist	

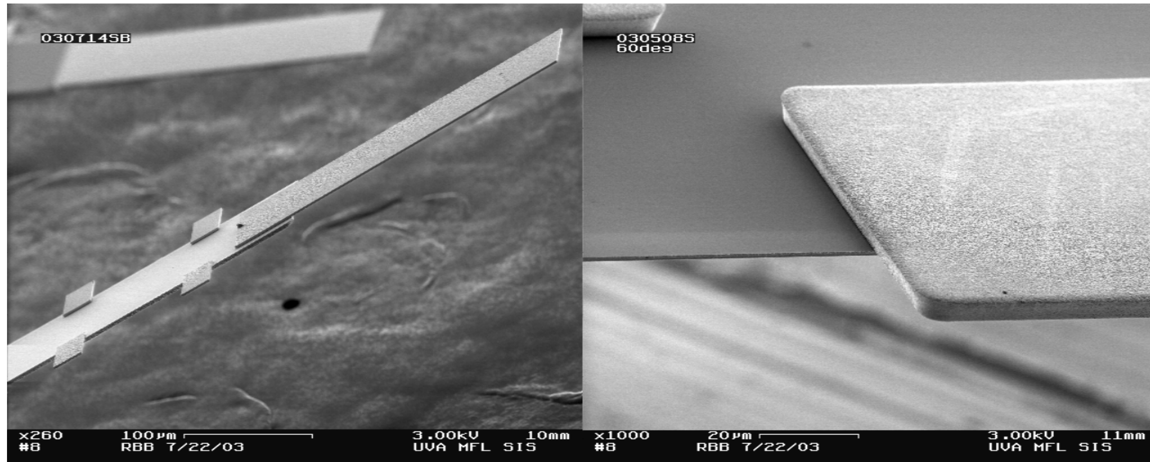

Figure 3. At left is an image of a 4um thick silicon chip with 1.5um thick gold beam leads of various lengths protruding from the perimeters. The longest beam lead extends 260um beyond the edge of the silicon. The right image shows a 1.6um thick chip with 4.5um thick beam leads.

Adhesion of the gold beam leads to the silicon chips is found to be excellent; none of the chips observed in the seven cases were found to be missing any beam leads. The successful adhesion is attributed to the 10nm thick titanium adhesion layer that is deposited prior to the seed layer gold. Figure 3 shows two SEM micrographs of completed beam lead chips. The micrographs are taken with the chips positioned at a high angle in order to show the profile of the ultra-thin silicon and gold beam leads.

As a demonstration of the durability of the beam leads and the silicon chips, we placed the chips within 100nm wide microchannels and compressed the beam leads along the channel shoulder. The microchannels were diced into a silicon wafer using a dicing saw. A chip was then gently placed within the microstrip channels using a pair of tweezers. The beam leads supported the chips along the length of the chip. A glass slide was then placed on top of the microchannel, and then clamped down to simulate the force associated with the clamping of two receiver block halves. Using a clear glass plate to simulate the upper block half allowed the beam leads to be observed as pressure was applied. The beam leads, 1.5um thick in this case, supported the chip through the experiment and did not tear of break away from the silicon chip. A photograph of a chip in the microstrip channel is shown in Figure 4.

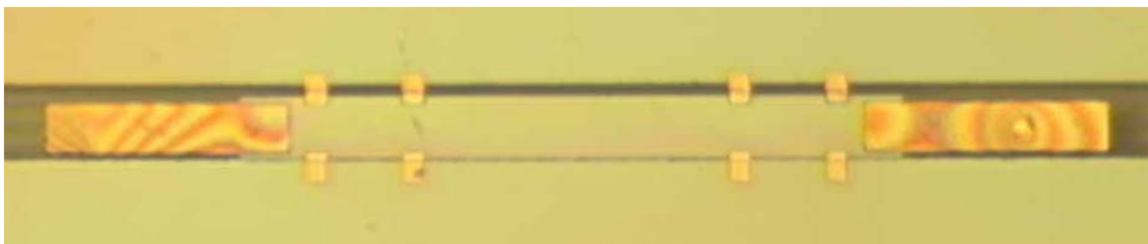

Figure 4. A 4um thick silicon chip with 1.5um thick gold beam leads placed within a microstrip channel. A glass slide is clamped over top of the sample in order to simulate the pressure associated with compressing the beam leads between the two halves of a receiver block. The glass slide allows for the gold beam leads to be observed as pressure is applied.

4. Conclusion

We have developed a new process for fabricating ultra-thin silicon chips with gold beam leads extending from the perimeters from SOI wafers. Chip thickness ranges from 1.6um to 4um. Beam leads were plated onto all of these chips to thickness between 1um and 4.5um, and are mechanically rigid enough to be handled with tweezers and compressed within a microstrip channel.

RF simulations show that such chips are useful for superconducting SIS and HEB THz receiver applications. We have separately fabricated working niobium based HEB bolometers on SOI wafers [9]. In addition, receiver design, machining and assembly of THz superconducting receivers is greatly simplified. Superconducting circuits with beam lead RF and IF connections ease the assembly of receivers since the electrical connections to the chip need not be wire bonded, soldered or connected via gaskets or micro-springs. Beam leads make it possible to quickly test receiver components, and to discard non-functioning elements without having to replace entire arrays.

Acknowledgements

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